Page NO.

1. 1 to 117 – Mid Term + Final Term

MD IFTAKHAR KABIR SAKUR

25th BATCH

COMPUTER AND COMMUNICATION ENGINEERING

International Islamic University Chittagong

COURSE CODE: CCE-1203

COURSE TITLE: Basic Electronics

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Second Semester Starts From Next Page

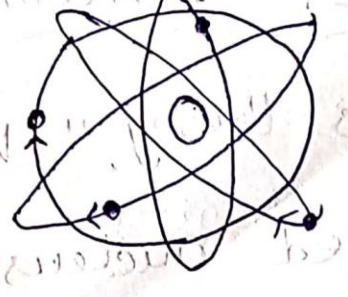
CCE-1203

Structure Of an Atom

→ According to Bohr's theory, "the Atom Consists Of positively charged nucleus and a number of negatively charged electrons which revolve round the nucleus in various ~~ord~~ Orbits.

• According to Bohr's model, an electron is said to be moved in a orbit, whereas according quantum mechanics an electron is said to be somewhere in free space of the atom, Called as Orbital.

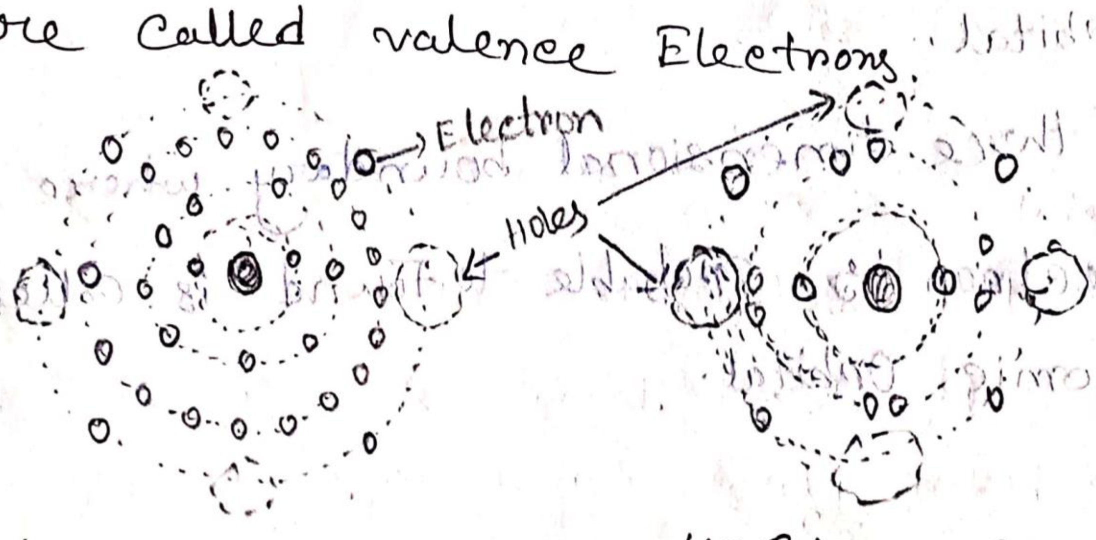
A three dimensional boundary where an electron is probable to found is called as Atomic Orbital.



[F] Valence Shell & Valence Electron:-

Electron can occupy only certain orbital rings or shells at fixed distances from the nucleus and that each shell can contain only a particular number of electrons.

- The outermost shell is called valence shell and the electrons in this shell are called valence Electrons.



(a) Germanium Atom (b) Silicon Atom

Concepts of Holes:-

- Each atom has a maximum of 4 electrons in their valence shell when they can contain a maximum of 8.
- It is said that, the valence shell has 4 electrons & 4 holes.
- A hole can be defined easily as an absence of an electron in a shell where one could exist.

Energy Level:-

- Each shell has an energy level associated with it.
- The closer a shell is to the nucleus, the stronger are the forces that bind it.
- Energy level represents the amount of energy that would have to be supplied to extract an electron from the shell.

• Energy levels are measured in Electron volts. It is defined as the amount of Energy required to move one electron through a potential difference of one volt.

Energy Bands:-

In gaseous substances, the arrangement of molecules is not close.

In liquids the molecular arrangement is moderate.

But in solids, the molecules are so closely arranged, that the electrons in the atoms of molecules tend to move into the Orbitals of neighboring atoms.

• Due to intermixing of atoms in solids, instead of single energy levels, there will be bands of energy levels formed. These set of energy levels, which are closely packed are called as Energy bands.

Why should there be Energy Bands:-

Electrons carry a single electronic charge & have a spin of $\frac{1}{2}$. This implies that they are fermions, particles which obey the pauli exclusion principle.

- The pauli exclusion principle states that two fermions can occupy the same quantum state described by a complete set of quantum numbers.

⇒ Every electron will have a specific energy associated with it.

একেকটা electronic shell-এ যে কয়টা electron থাকবে সে কয়টা Energy level। আর সবগুলো Energy Level মিলে হয় Energy Band।

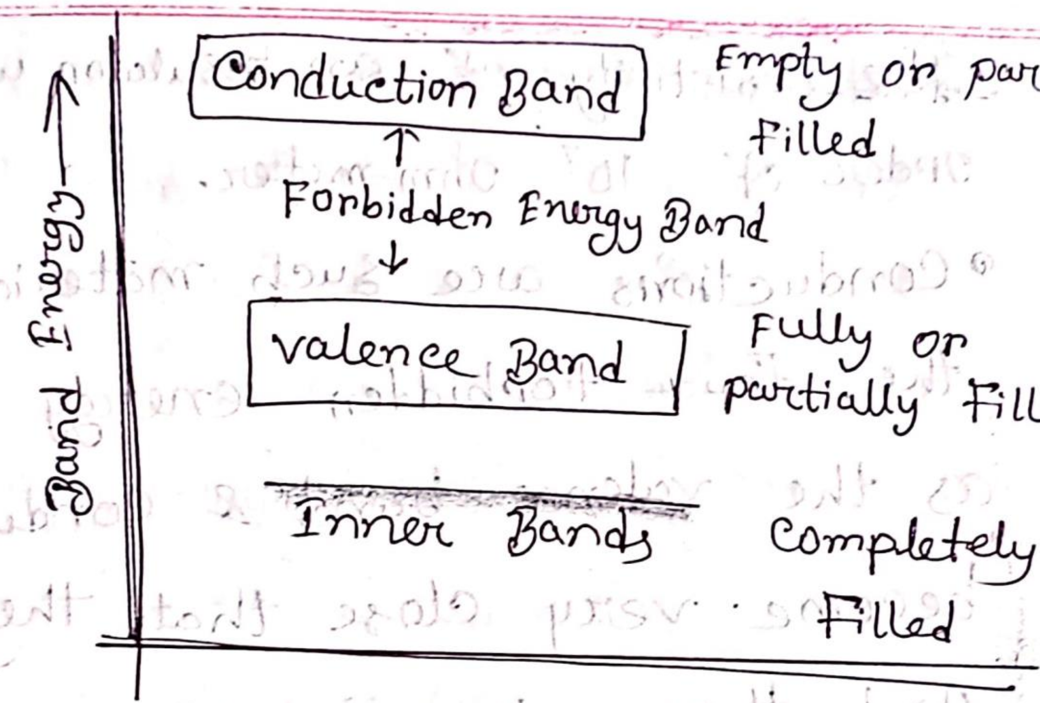
[1] Bands within Energy Band (Valence Band):-

The valance electrons in the valence Shell, containing a series of energy levels, form an energy band which is called Valence Band.

- The valence electrons are so loosely attached to the nucleus that even room temperature, few of valence electrons leave the band to be free. These are called as free electrons as they tend to move towards the neighboring atoms.

- These free electrons are the ones which conduct (ব্যাপার) the current in a conductor and hence called as Conduction (পরিবহন) Electrons.
- The band which contains conduction electrons is called as conduction band.

The conduction band is the band having the lowest occupied energy.



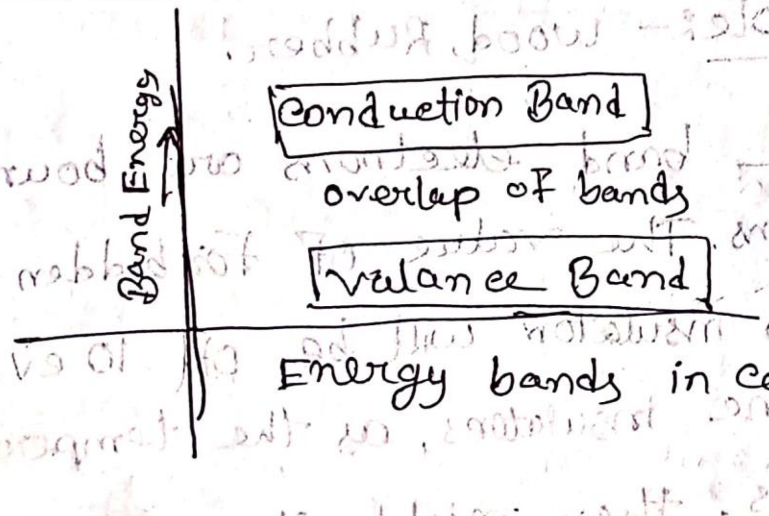
Materials according to Energy Bands (Insulator):

- Insulators (অন্তরক) are such materials in which the conduction can't take place, due to the large Forbidden gap.
- Example:- wood, Rubber.
- Valence band electrons are bound tightly to atoms. The value of Forbidden energy gap for an insulator will be of 10 ev.
- For some insulators, as the temperature increases, they might show some conduction.

- The resistivity of an insulator will be in the order of 10^7 ohm-meter.
- Conductions are such materials in which the ~~Ford~~ Forbidden energy gap disappears as the valence band & conduction band become very close that they overlap. And there the forbidden gap in a conductor doesnot exist.

Example:- Copper, Aluminum.

- A slight increase in voltage, increase the conduction.



Energy bands in conductors.

• Semiconductors are such materials in which the Forbidden energy gap is small and the Conduction takes place if some external energy is applied. The Forbidden energy gap is ~~s~~ very small. Example:- Silicon, Germanium.

• A semiconductor is neither an insulator nor a good ~~calculator~~ conductor. As the temperature increases, the conductivity of a semiconductor increases. The Conductivity of a semi-conductor will be in the order of 102 ~~mho~~ mho-meter.

অর্ধ পরিবাহীর জন্য Ohm's Law প্রযোজ্য না।

⊞ Conduction in Semiconductors:-

• Both valence electrons combine to form "Electron pairs". This bonding is not so very strong & hence it is a covalent bond.

Example: Germanium which has 4 valence electron.

Covalent :- সমযোজী বন্ধন

4. Hole current :-

When a covalent bond is broken, a hole is created. Actually there is a strong tendency of semiconductor crystal to form a covalent bond.

- An electron, when gets shifted from a place a hole is formed.

(A) • ⟶ o (B) o (C)

(A) o ⟶ • (B) ⟶ o (C)

(A) • ⟶ o (B) ⟶ • (C)

এই Flow কে বলা হয় hole current

⇒ This movement of hole in the absence of an applied field is random (এলোমেলো). But, when electric field is applied, the hole drifts (স্রোতে) along the applied field, which constitutes the hole current.

This is called hole current but not electron current, because the movement of holes contributes the current flow.

Temperature এর effect velocity এর উপর electron এর অস্তিত্ব এর উপর নয়।

Conductor এ যত temperature বাড়াই তত কমে current এর flow।

⇒ Due to the thermal energy supplied to the crystal, some electrons tend to move out of their place & break the covalent bonds. These broken covalent bonds, result in free electrons which wander randomly. But the moved away electrons creates an empty space or valence behind, which is called as a hole.

- The hole is a unit positive charge & electron is a unit negative charge. The liberated electrons move randomly but when some external electric field is applied, these electrons move in opposite direction to the applied field. But the holes created due to absence of electrons, move in the direction of applied field.

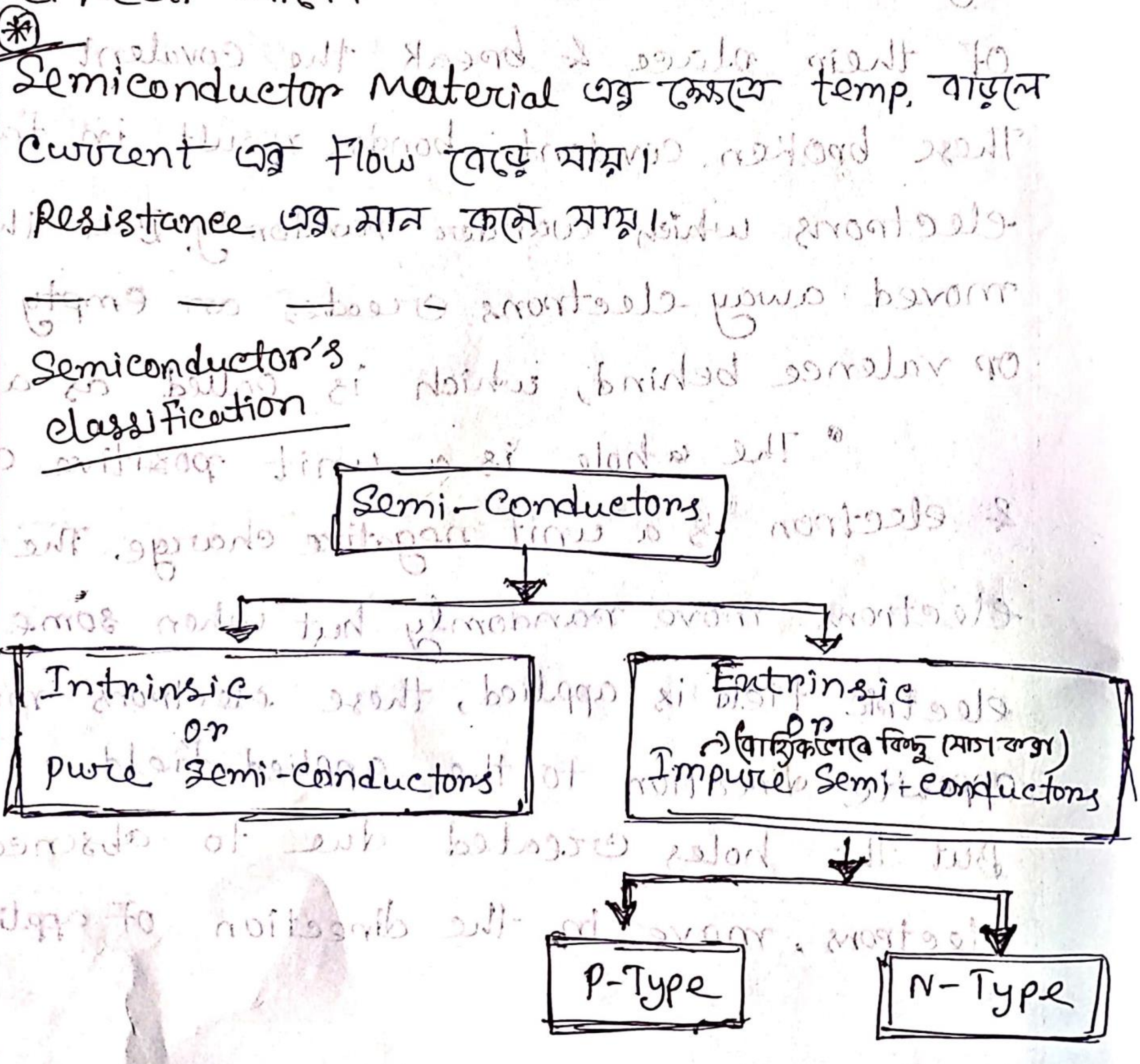
[Temperature coefficient বলা হয়। resistance এর জন্য বলা হয়]

Negative Temperature Coefficient:-

* Temp. বাড়লে electron এর সংখ্যার উপর কোনো effect আসে না বরং এর Flow এর উপর effect আসে।

* Semiconductor Material এর ক্ষেত্রে temp. বাড়লে current এর Flow বেড়ে যায়। Resistance এর মান কমে যায়।

Semiconductor's classification



13th February, 2021

Saturday

Intrinsic Semiconductor
(স্বৰকাত অৰ্ধ-পৰিবাহী)

→A semi-conductor in its extremely pure form is said to be an intrinsic semiconductor.

· The electrons & holes are created by thermal excitation. The number of free electrons is equal to the number of holes. The conduction capability is small at room temperature

Extrinsic Semiconductor
(অস্বৰকাত অৰ্ধ-পৰিবাহী)

In order to increase the conduction capability of intrinsic semiconductor, it is better to add some ~~imput~~ impurities. This process is called as Doping.

This droped intinsic semi-conductor is called as an Extrinsic Semiconductor.

There are two types of impurity:-

(1) pentavalent Impurities:-

→(পঞ্চযোজী) →(5টি electron)

The pentavalent impurities are the ones which has five valence electrons in the outer most orbit.

The pentavalent atom is called as donor atom, cause it donates one electron to the conduction band of pure semi-conductor atom. Example:- Bismuth, Antimony, Arsenic, Phosphorus.

→(ত্রিযোজী)

2) Trivalent Impurities:-

The ones which has three valence electrons in the outer most orbit.

It is called as an acceptor atom because it accepts one electron from the semiconductor atom.

Example:- Galium, Indium, Aluminum, Boron.

N-Type Extrinsic Semiconductor:-

(Access electron তৈরি হওয়ায় এই ধরনের Semi-Conductor Material কে N-type semiconductor Material বলে)

⇒ A small amount of pentavalent impurity is added to a pure semiconductor to result in N type extrinsic semiconductor. The added impurity has 5 valence electrons.

Example:- IF (As) atom is used to the ~~(ge)~~ (Ge) atom, four of the valence electrons get attached with the (Ge) atoms while one electron remains as a free electron.

All these free electrons constitute electron current. When, the impurity added to pure semiconductor provides electrons for conduction. As the conduction takes place through electrons, the electrons are majority carriers & the holes are minority carriers.

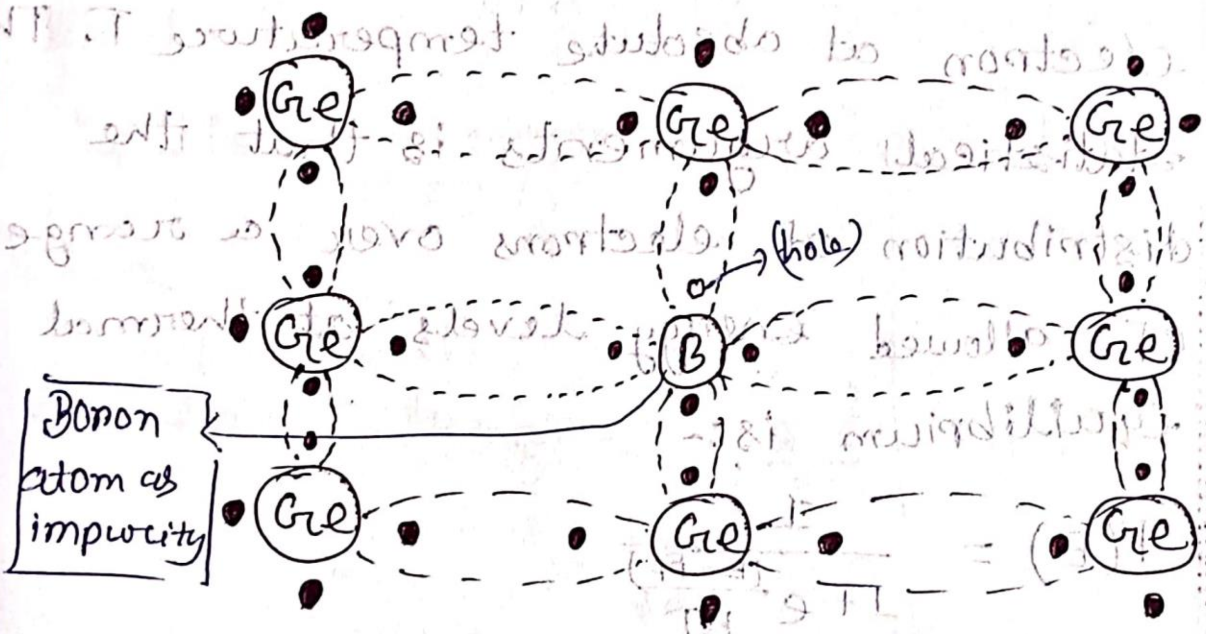
• When an electric field is applied to an N-Type semiconductor, to which a pentavalent impurity is added, the free electrons travel towards positive electrode. This is called as a negative or N-type conductivity.

P-Type Extrinsic Semiconductor

A small amount of trivalent impurity is added to a pure semiconductor to result in p-type extrinsic semiconductor. The added impurity has 3 valence electrons.

If a Boron atom is added to the germanium atom, three of the valence electrons get attached with the Ge atoms, to form three covalent bonds. But one more electron in germanium remains without forming any bond.

As there is no electron in Boron remaining to form a covalent bond, the space is treated as a hole.



PDF

Math Formula

Density of states and Fermi Dirac Function:-

The Function PDF F(E).

The probability that an available energy state at E will be occupied by an electron at absolute temperature T. The statistical arguments is that the distribution of electrons over a range of allowed energy levels at thermal equilibrium is:-

$$F(E) = \frac{1}{1 + e^{\frac{(E - E_F)}{KT}}}$$

Here,

K is Boltzman's constant ($k = 8.62 \times 10^{-5}$ eV/K or, $k = 1.38 \times 10^{-23}$ J/K)

The quantity E, is called the Fermi level.

T = Temperature

Fermi Level:-

এটা এমন একটা state, যে state এ electron থাকার probability 50-50।

Cause,

$E = E_F$ হলে,

$$F(E_F) = \frac{1}{1+e^{\frac{(E_F-E_F)}{K\cdot T}}} = \frac{1}{1+e^0} = \frac{1}{1+1} = \frac{1}{2}$$

when,

$T=0$ & $E > E_F$ then,

$$F(z) = \frac{1}{1+e^{\frac{+\cdots}{0}}} = \frac{1}{1+e^{\alpha}} = \frac{1}{1+\alpha}$$

$$= \frac{1}{\alpha} = 0$$

$\therefore F(z) = 0$.

when, $E < E_F$ then,

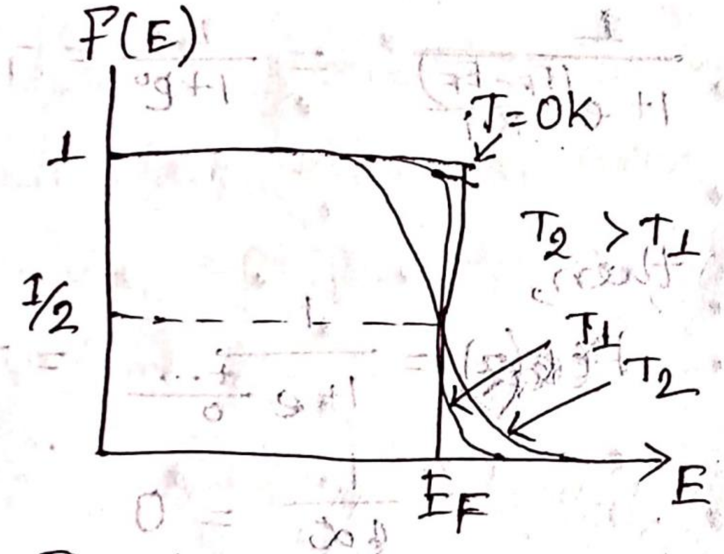
$$F(z') = \frac{1}{1+e^{\frac{-\cdots}{0}}} = \frac{1}{1+e^{-\alpha}}$$

so, $= \frac{1}{1+0} = \frac{1}{1} = 1$

$F(z') = 1$.

☐ Fermi Level Conduction ও valence band এর মাঝামাঝি থাকে।

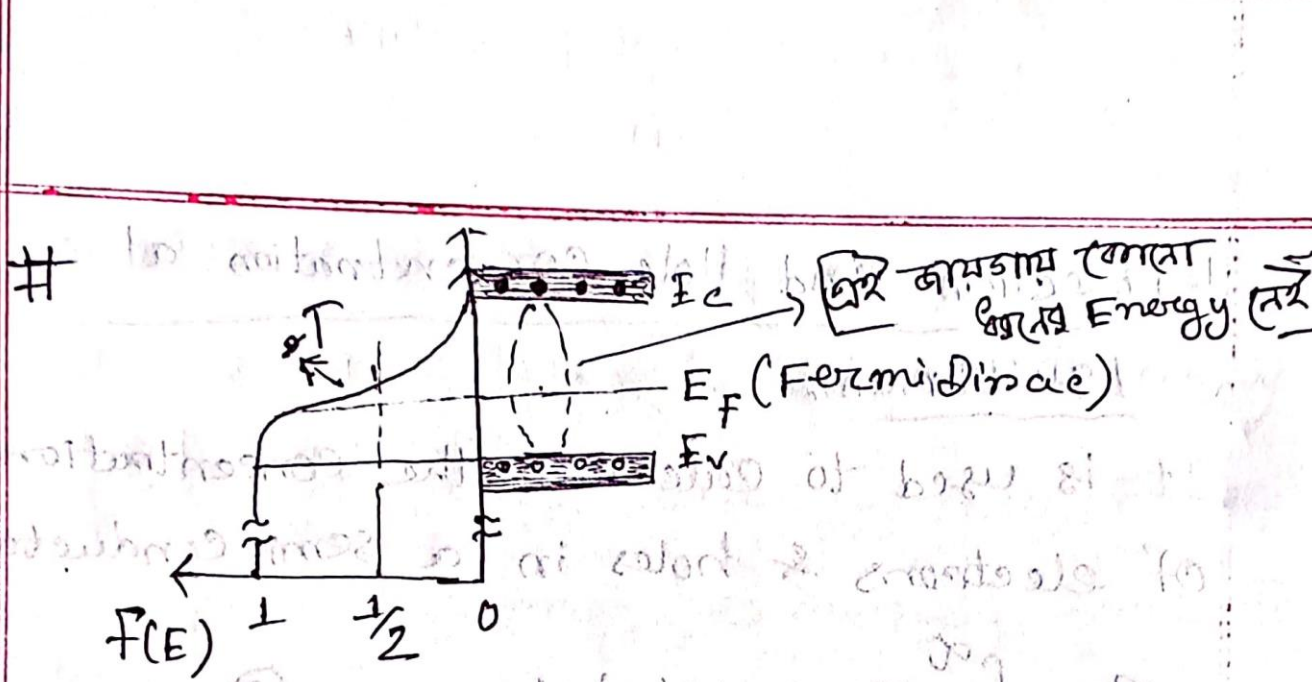
It means কোনো Temperature দেওয়া না হলে Intrinsic semi-conductor এর ক্ষেত্রে কোনো electron পাওয়ার সম্ভাবনা নেই।



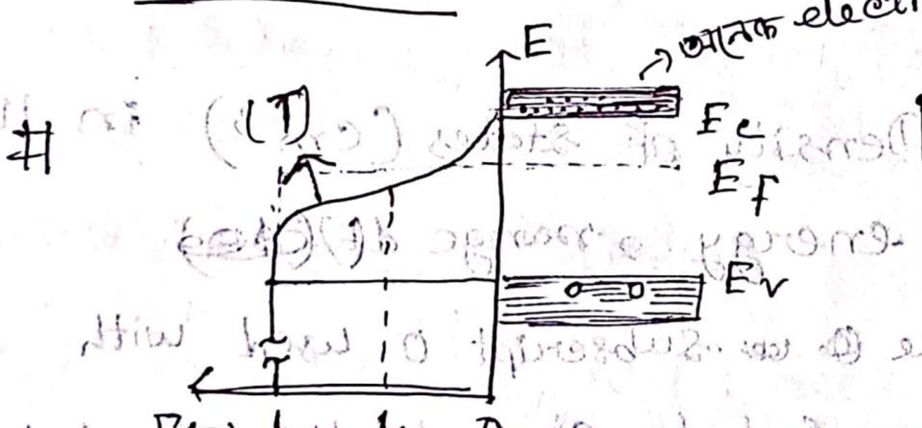
Ex:- The Fermi Dirac Distribution Function.

☐ Fermi Dirac Dist. Applied to Semiconductor:-

Intrinsic -এর ক্ষেত্রে Conduction Band যে পরিমাণ electron থাকবে valence Band এ সে পরিমাণ hole থাকবে।



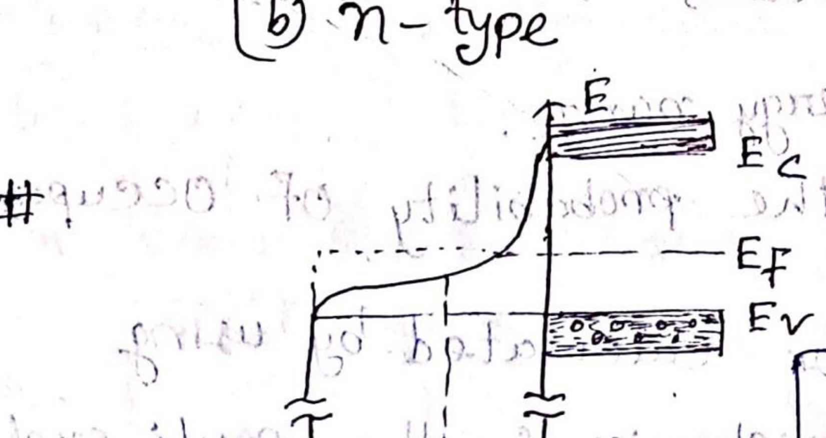
(a) Intrinsic



E_c ও E_F এর মধ্যে Energy এর Difference যত কমবে ততই Free electron এর সংখ্যা বাড়বে vice-versa

(b) n-type

$E_F - E_V$ এর পার্থক্য যত কম তত hole তত কম।



The value of $E_c - E_F$ gives a measure of n (electron concentration)

The value $(E_F - E_V)$ indicates how strongly P-type material is.

(c) P-Type

Electron and Hole concentration at Equilibrium:-

It is used to calculate the concentrations of electrons & holes in a semi-conductor

$$n_0 = \int_{E_F}^{\infty} F(E) \cdot N(E) \cdot dE \quad \text{—— (2)}$$

Here,

$N(E)$ = Density of states (cm^{-3}) in the energy range dE

n_0 = The subscript 0 used with the electron & hole concentration symbols (n_0, P_0) indicates equilibrium conditions.

dE = The energy range.

$F(E)$ = The probability of occupancy.

$N(E)$ can be calculated by using quantum mechanics & the pauli exclusion principle.

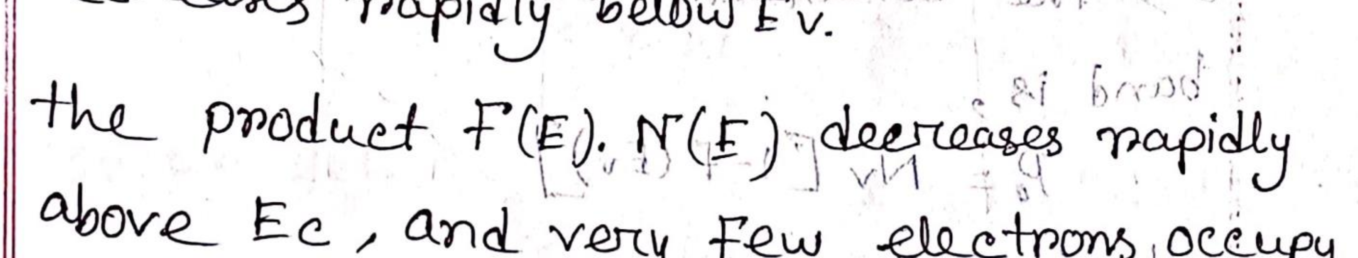
N(E) is proportional to $E^{0.5}$.

The Fermi Function becomes extremely small for large energy. Also, Fermi Function becomes extremely small for large energies.

The probability of finding an empty state (hole) in the valence band [1-F(E)] decreases rapidly below Ev.

the product F(E). N(E) decreases rapidly above Ec, and very few electrons occupy energy states far above the conduction band edge.

[E] Conduction Band এর width দিয়ে electron সংখ্যা বের করা যায়



$F(E_v)$ = Occupied হওয়ার Probability সংখ্যা।

The probability OF occupancy at Ec.

$$n_0 = N_c F(E_c)$$

Here,

N_c = Conduction Band এর width এ কতটা Energy state available আছে তা

Hole এর ক্ষেত্রে:-

$$N(E)\,[1 - F(E)]$$

So, The concentration of holes in the valence band is,

$$P_0 = N_v\,[1 - F(E_v)]$$

Here,

N_v = Valence Band এর Total Energy state এর সংখ্যা

$1 - F(E_v)$ = Occupied না হওয়ার Probability সংখ্যা।

*** Note

→ N-Node দিয়ে total electron

→ P-Node দিয়ে total hole এর সংখ্যা বের করতে পারব।

কোনো একটি N-type ও P-type Material কে Doping করার পর total electron Density কত এবং Hole এর Density কতটুকু এটা বের করতে পারাই উপরোক্ত ~~অবস্থা~~ equation গুলোর উদ্দেশ্য। কারন এর উপর Depend করে Conductivity বের করা যায়। অর্থাৎ কে কতটুকু current conduct করতে পারে তা বের করা যাবে।

$$\Rightarrow f(E_c) = \frac{1}{1+e^{(E_c-E_F)/KT}} \simeq e^{-(E_c-E_F)/KT}$$

So, we get,

$$n_o = N_c \, e^{-(E_c-E_F)/KT} \quad \text{——— (23)}$$

(Total electron)

Total available effective density of states,

$$N_c = 2\left(2\pi m_n KT/h^2\right)^{3/2}$$

যদি N_c, E_c ও E_F দেওয়া থাকে তবে যেকোনো material এর জন্য electron সংখ্যা বের করা সম্ভব।

P-Type এর জন্য,

$$1-F(E_v) = 1 - \frac{1}{1+e^{(E_v-E_F)/KT}}$$

$$= e^{-(E_F-E_v)/KT}$$

Cause, $E_v < E_F$ হয়

Intrinsic semi-conductor এর ক্ষেত্রে electron এর সংখ্যাঃ-

$$n_i = N_c e^{-(E_c-E_F)/KT}$$

$$p_i = N_v e^{-(E_i-E_v)/KT} \quad \text{---} (5)$$

The product of n_0 & p_0 at equilibrium,

$$n_0 p_0 = \left(N_c e^{-(E_c-E_F)/KT}\right) \cdot \left(N_v e^{-(E_F-E_v)/KT}\right)$$

$$= N_c \cdot N_v \cdot e^{-(E_c-E_v)/KT}$$

$$= N_c \cdot N_v \cdot e^{-E_g/KT} \quad \text{---} (6)$$

এইখানে কোনো Constant Temperature -এ n ও p এর গুণফল always constant হয়।

P-Type এর জন্য,

$$1-F(E_v) = 1 - \frac{1}{1+e^{(E_v-E_F)/KT}}$$

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$$n_i p_i = \left(N_c e^{-(E_c - E_i)/KT}\right) \cdot \left(N_v e^{-(E_i - E_v)/KT}\right)$$

$$= N_c \cdot N_v e^{-E_g/KT} \quad \text{—— (7)}$$

☐ Electron conductivity of a metal :-

The actual relation is $v = \mu_e E$ [কোনো electric Field দিলে electron কি পরিমাণ move করে তার মান]

Let, e = electron charge (coloumb)

v = velocity of electron

$I = nAqv$

A = Cross section Area

q = Charge of electron.

v = velocity.

n = Amount of total electron.

Or, $I = neA\mu_e E$ [কোনো তারের মধ্য দিয়ে যাওয়া total current]

Also, $E = V/l$. [V = voltage]

অতএব, $R = \frac{V}{I} = \frac{l}{A}\left(\frac{1}{ne\mu_e}\right) = \rho \cdot \frac{l}{A}$

So, resistivity, $\rho = 1/ne\mu_e$; ohm-m

Conductivity, $\sigma = ne\mu_e$; siemens/m

Conductivity of Intrinsic Semiconductors:

p_i = Density of holes in an Intrinsic semi-conductor (per m^3)

e = electron charge (coulomb)

A = Cross-section of the semiconductor (m^2)

Since in an Intrinsic semiconductor,

$$n_i = p_i$$

$$I = n_i e (v_e + v_h) A$$

$$= n_i e (\mu_h + \mu_e) EA$$

Here, μ_e = electron mobility $= v_e/E$

μ_h = hole mobility $= v_h/E$

So, $I = n_i e(\mu_e + \mu_h) AV/l$

$$V/I = l/A \cdot \frac{1}{n_i e(\mu_e + \mu_h)} = \rho_i \cdot \frac{l}{A}$$

So, resistivity of semiconductor,

$$\rho_i = \frac{1}{n_i e(\mu_e + \mu_h)} \text{ ohm-m}$$

The electrical conductivity which is the reciprocal of resistivity is given by,

$$\sigma_i = n_i e(\mu_e + \mu_h) \text{ S/m}$$

#

So, current density $J = I/A$

(electron mobility → μ_e, hole mobility → μ_h)

$$\therefore J = n_i e(\mu_e + \mu_h)E = \sigma_i E$$

$$\therefore \sigma_i = J/E$$ [এটাকে current এর ক্ষেত্রে Ohm's law বলে]

So, conductivity of semiconductors depends on two factors

(i) number of current carriers present per unit volume.

(ii) The mobility of the current carriers.

[F] Conductivity of Extrinsic Semiconductors:-

(অর্থাৎ, যেকোনো Material এর ক্ষেত্রে)

$$\sigma = (n e \mu_e + p e \mu_h) E$$

Here, ne = Number of electrons

μ_e = Mobility of electrons

pe = Charge of holes

μ_h = Mobility of holes

(a) N-type Extrinsic semi-conductor:-

$$J_n = e(n_n \mu_e + P_n \mu_h) E$$

(b) P-Type:-

$$J_P = e(n_P \mu_e + P_P \mu_h) E$$

But, N-type Materials-এ electron এর সংখ্যা hole এর ~~অ~~ সংখ্যা হতে অনেক অনেক বেশি।

$$n_n >> P_n$$

So, we can write,

$$J_n = n_n e \mu_e E$$
$$\sigma = n_n e \mu_e$$

& in

$$J_P = P_P e \mu_h E$$
$$\sigma_P = P_P e \mu_h$$

Drift:-

Semiconductor যে কারনে Flow করে current এর তার কারন হলো:-

(i) ~~charge~~ electron (voltage source connect এর মাধ্যমে electron ও hole এর movement — এদের Drift current বলে)

(ii) ~~hole~~ voltage source connect ছাড়া automatically বেশি ঘনত্ব থেকে কম ঘনত্বের জায়গায় current এর Flow

⊛ Charge drift under the influence of applied electric field

⊛ Diffusion of charge from a region of high charge density to one of low charge density.

⊛ Current Density due to hole diffusion:-

⇒ Current Density due to hole diffusion,

$$J_h = -e D_h \, dp/dx$$

D_h = electron ও hole এর diffusion (গুণ) constant

Current Density due to ~~curre~~ electron diffusion:-

$$J_e = e D_e \cdot dn/dx$$

e হলো charge, $= 1.6 \times 10^{-19}$

⊛ dn/dx or dp/dx = charge career এর Density কি হারে পরিবর্তন হচ্ছে তা।

⊡ Combined Drift & Diffusion currents:-

~~for Drift~~

$$J_e = e\mu_e n E + e D_e \frac{dn}{dx} \; A/m^2$$

$e\mu_e n E$ = Drift current; $e D_e \frac{dn}{dx}$ = Diffusion current

$J_h = e\mu_h pE - eD_h \, dp/dx \; Am^{-2}$

Drift current — Diffusion current,

Relation Between D & μ:-

$\mu_e = \frac{e}{KT} \cdot D_e$

$\mu_h = \frac{e}{KT} \cdot D_h$

or, $\frac{D_e}{\mu_e} = \frac{D_h}{\mu_h} = \frac{KT}{e} = \frac{T}{11,600}$

This relationship is known as Einstein equation,

$t = 23°c$, $T = 300°K$

$D/\mu = 300/11,600 = 1/39$ or, $\mu = 39D$

Recombination:-

The process is essentially the return of a free conduction electron to the valence band and is accompanied by the emission of energy.

Apart from drift and diffusion, a third phenomenon which occurs in semiconductors is called recombination. That result from the collision of an electron with a hole.

Math Solution:-

51.10 Silicon is doped with acceptor atoms to a density of $10^{22} m^{-3}$. If it is assumed that all acceptor centres are ionized, calculate the conductivity of the extrinsic silicon. Given that, intrinsic density is $1.4 \times 10^{16} m^{-3}$; $\mu_e = 0.145 m^{-3}$ and $\mu_h = 0.05 m^{-3}$.

Ans:- (এটি N-type Material)

The minority carrier density can be found ~~from~~ $np = n_i^2$

Now, $p = 10^{22}$ ∴ $n \times 10^{22} = (1.4 \times 10^{16})^2$

∴ $n = 1.96 \times 10^{10} / m^3$

Now,

$$\sigma = ne\mu_e + pe\mu_h$$

$$= 1.96 \times 10^{10} \times 0.145 \times 1.6 \times 10^{-19} + 10^{22} \times 0.05 \times 1.6 \times 1.6 \times 10^{-19}$$

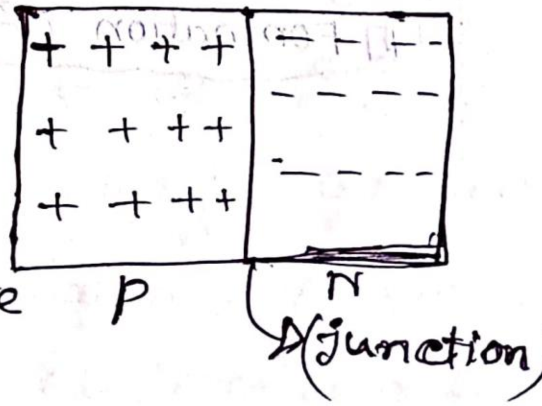
$= 80$ S/m

(Ans)

Diodes:

~~P & N-type~~ It is a single piece of a semiconductor material half of which is doped by P-type impurity and the other half by N-type impurity.

The plane which dividing the two zones is called Junction. The P-N junction is fundamental to the operation of diodes, transistors & other solid-state devices.



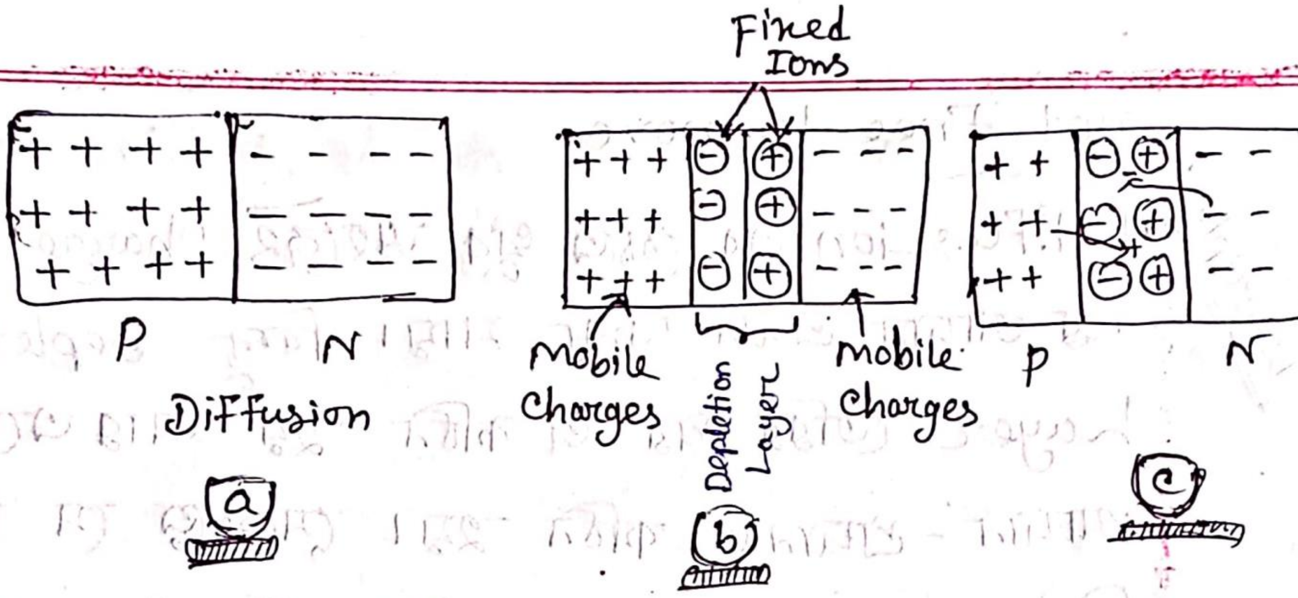
If anything unusual happens at the junction. It is found that three phenomena take place:-

1) A thin depletion (ह्रास कक्षा) layer or region (also called space-charge region or transition region) is established on both sides of the junction and is so called because it is depleted of free charge carriers. Its thickness is about 10^{-6} m.

2) A barrier potential or junction potential is developed across the junction.

3) The presence of depletion layer gives rise to junction capacitances & diffusion (विसरण) capacitances.

Formation of Depletion Layer:-



⇒ Holes are in p-region & electrons are in N-region. However, there are greater concentration of holes in p-region than in N-region. Concentration of electrons is greater in N-region than in p-region (where they exist as minority carriers).

This differences establishes density gradient across the junction resulting in carrier diffusion. So, Holes diffuse ~~to~~ from p to N-region & electrons from N to p-region & terminate their existance by recombination. Free & Mobile charge carriers like electrons & holes there being present only positive ions which are

Description:-

not Free to move.

• Diffussion এর ক্ষেত্রে খুব সহজেই charge ও hole এর আদান প্রদান করা যায়। কিন্তু Depletion Layer তৈরির পর তা কঠিন হয় আর এদের আদান - প্রদান ও কঠিন হয়। সেক্ষেত্রে যে বিভব নিয়ে আদান প্রদান করে তাকে Barrier potential বলে।

Barrier potential বের করার সূত্র:-

Silicon এর ক্ষেত্রে p-n জাংশন এর B.P হলো: 0.7 V

Germanium " " " " B.P " : 0.3 V

(Room-Temperature)

এই Barrier potential কোনো Charge Flow করতে দিবে না।

Summary:-

(i) Diffusion.

(ii) Depletion.

(iii) No Flowing of charge.

(−) → Acceptor atom

(+) → Donor atom

◻ @ Hole & electron এর মাঝে atom এর পার্থক্য:-

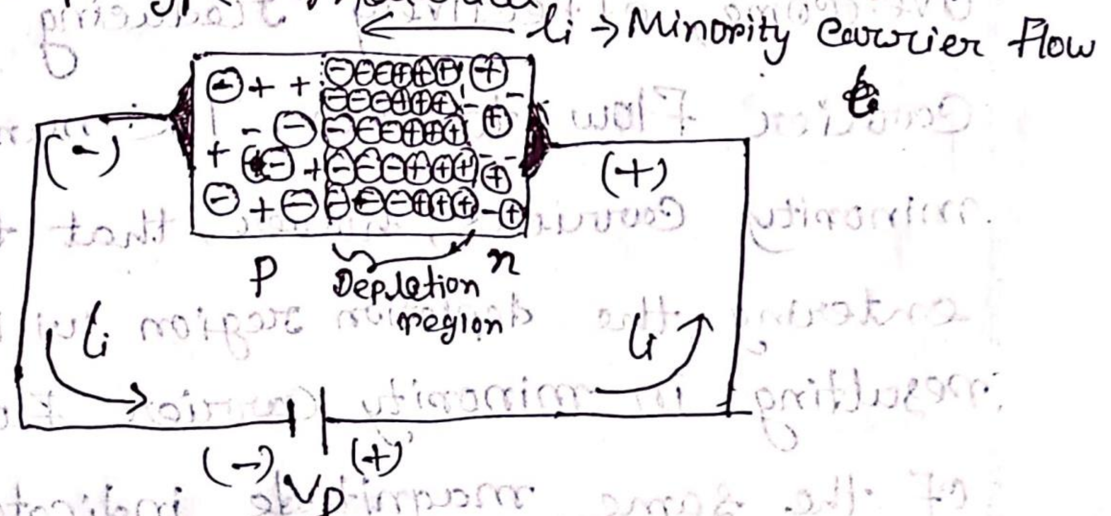
চার্জ carrier গুলো move করতে পারে,

atom গুলো move করতে পারেনা।

◻ Reverse Bias:-

উপরোক্ত সবকিছু NO Applied Bias ($V_D = 0$ Volts) এর অন্তর্ভুক্ত,

If an external potential of V volts is applied across the p-n junction such that positive terminal is connected to the n-type material & the negative terminal is connected to the p-type material.



The number of uncovered positive ions in the depletion region of the n-type material will increase due to the large number of "free" electrons drawn to the positive potential of the applied voltage.

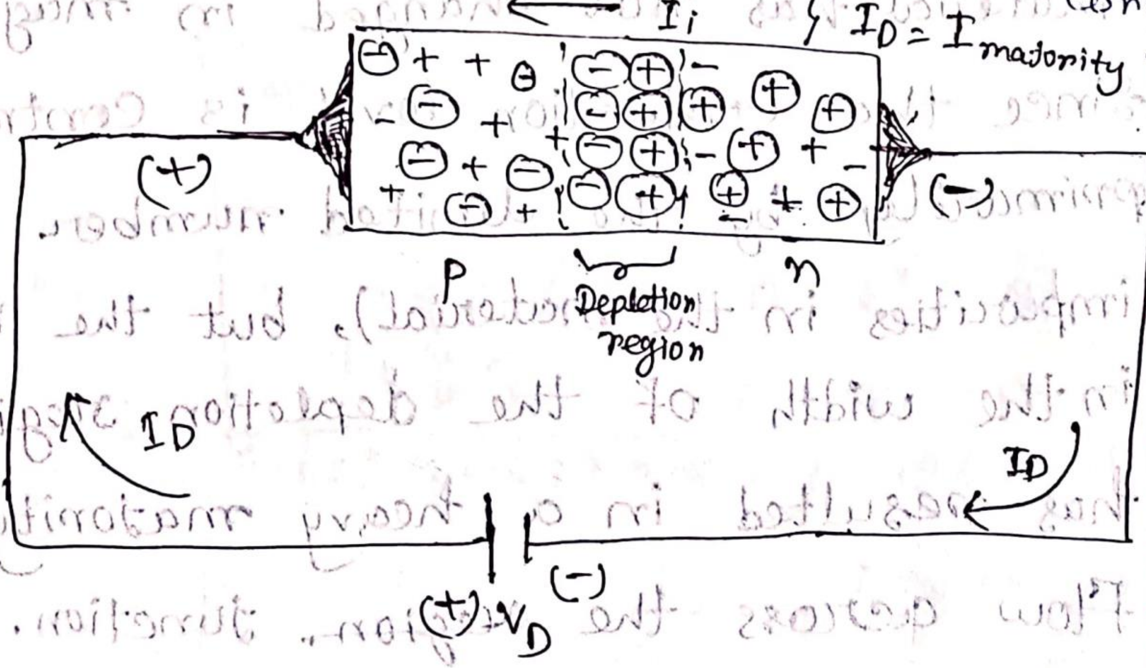
For similar reasons, the number of uncovered negative ions will increase in the p-type material.

The net effect, therefore, is a widening of the depletion region. The widening of the depletion region will establish too great a barrier for the majority carriers to overcome, effectively reducing the majority carrier flow to zero. The number of minority carriers, hower, that find themselves entering the depletion region will not change, resulting in minority carrier flow vectors of the same magnitude indicated with no applied voltage.

The current that exists under reverse-bias conditions is called the reverse saturation current & ~~step~~ is represented by I_r.

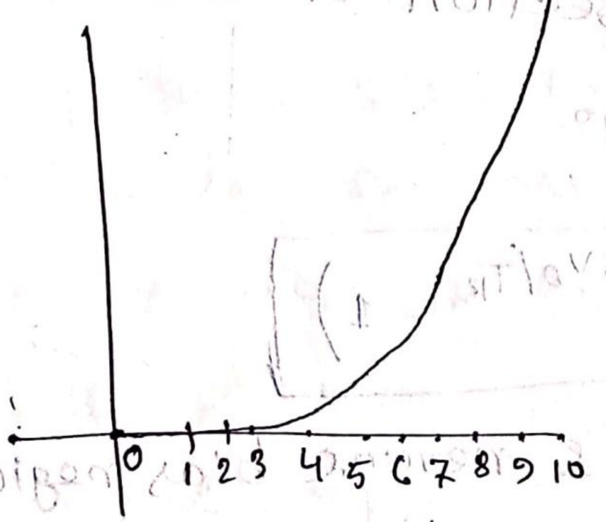
☐ Minority current এর Flow হওয়া থেমে গেলেই সেটা Saturation.

☐ Forward-Bias Condition (সবচেয়ে important Condition:-



V_D will "pressure" electrons in the n-type materials & holes in the p-type material to recombine with the ions near the boundary & reduce the width of the depletion region. The resulting minority carrier flow of electrons from the p-type materials to the n-type material (and of holes from the n-type to p-type material) has not changed in magnitude (since the conduction level is controlled primarily by the limited number of impurities in the material), but the reduction in the width of the depletion region has resulted in a heavy majority flow across the ~~region~~ junction.

An electron of the n-type material now "sees" a reduced barrier at junction due to the reduced depletion region & a strong attraction for the positive potential applied to the P-type material. As the applied bias increases in magnitude the depletion region will continue to decrease in width until a flood of electrons can pass through the junction.



□ I_S = reverse saturation current

$K = 11600/\eta$ with

$\eta = 1$ for Ge and

$\eta = 2$ for Si for relatively low levels of diode current (at or below the knee of the curve)

$\eta = 1$ for Ge & Si for higher level of diode current (in the rapidly increasing section of the curve)

$T_K = T_C + 273°$

$$I_D = I_S \left(e^{K V_D / T_K} - 1 \right)$$

I_D = Forward & reverse bias regions.

□ Zener Region:

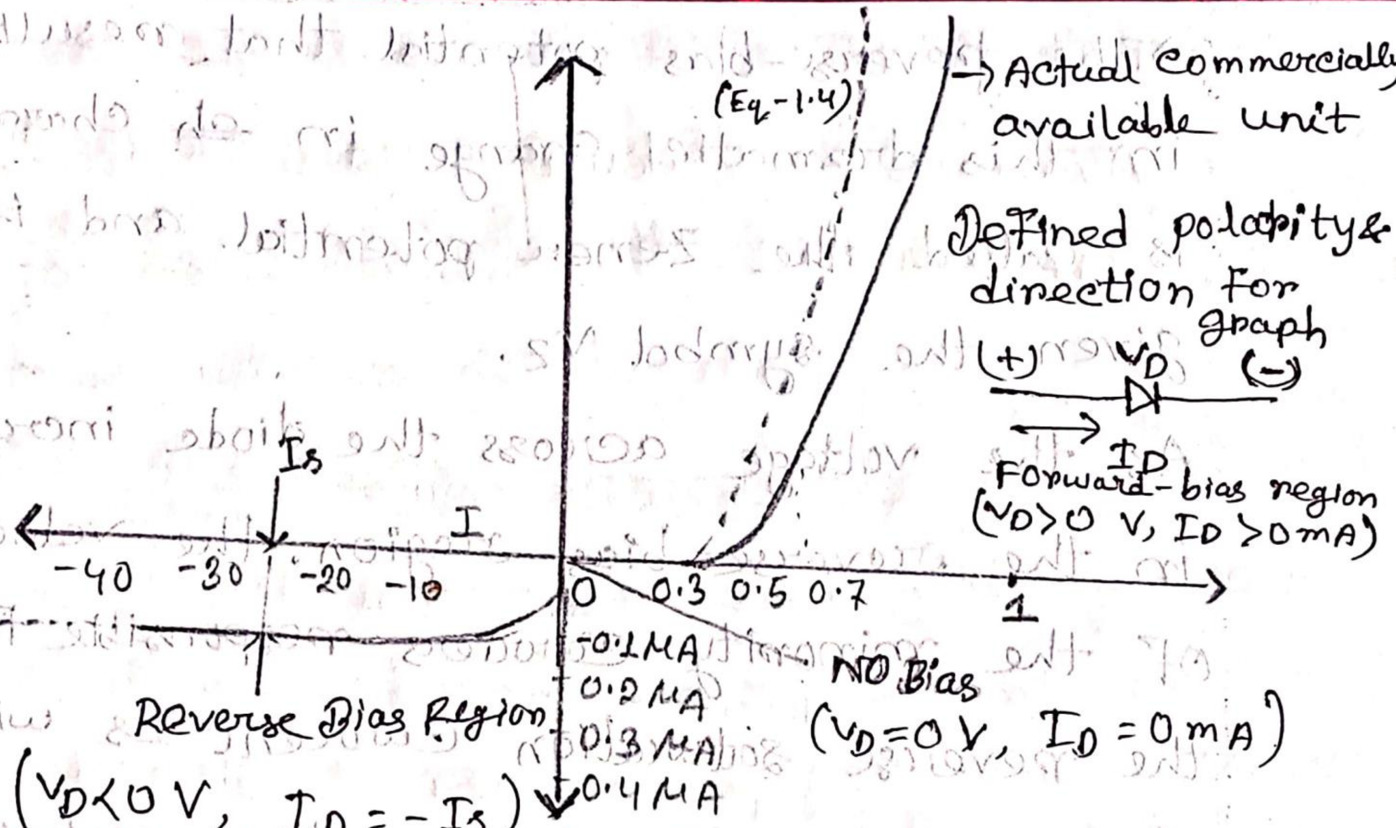
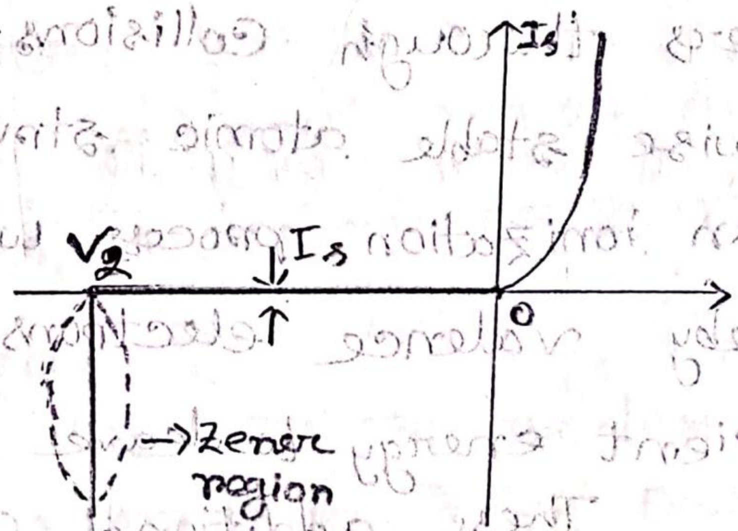


Figure1:- Silicon semi-conductor diode Characteristics

Figure02:-



⇒ The reverse-bias potential that results in this dramatic change in ~~ch~~ characteristics is called the Zener potential and is given the symbol V_Z.

As the voltage across the diode increases in the reverse-bias region, the velocity of the minority carriers responsible for the reverse saturation current I_s will also increase. Eventually, their velocity and associated kinetic energy ($W_K = \frac{1}{2}mv^2$) will be sufficient to release additional carriers through collisions with otherwise stable atomic structures. It's an ionization process will result whereby valence electrons absorb sufficient energy to leave parent atom.

These additional carriers can

then aid the ionization process to the point where a high avalanche current is established & the avalanche breakdown region determined.

(অধিক ভোল্টেজ প্রয়োগের দ্বারা Reverse-bias region এ বৃদ্ধি পায়। Minority carrier এর বেগ Reverse saturation current I_s এর জন্য ও বৃদ্ধি পায়। তাদের বেগ এবং গতিশক্তি গুলোর ফলে electron গুলোর বেগ বৃদ্ধি পায় এবং জোরে crystal এ আঘাত করে। এর ফলে crystal হতে electron গুলো মুক্ত অবস্থায় ছুটতে থাকে।

আর এই ঘটনাটাকেই বলা হয় Avalanche Breakdown) এবং process কে বলা হয় Avalance)

Zener Diode:-

Current Flow হবে reverse bias-এ আবার diode নষ্টও হবে না। এ ধরনের Diode কে বলা হয় zener diode।

B.V.C

Note:-

Avalance breakdown এর পরে Diode কে ব্যবহার করা যায় না। সেকারনে এই region এ কাজ করানো হয় না।

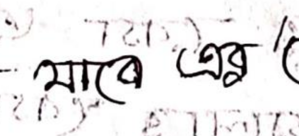
PRV rating:-

এটার মানে হলো কোনো Peak Reverse voltage। PRV লেখা থাকা মানে কোনো কিছুকে Reverse Bias-এ কোনো কিছু কে সর্বোচ্চ তত voltage দেওয়া যাবে এর থেকে বেশি দেওয়া হলে তা নষ্ট হয়ে যাবে।

Diode-এ voltage রেটিং দেওয়া থাকে।

Diode এর Resistance:-

একে তিনটি ভাগে ভাগ করা হয়।



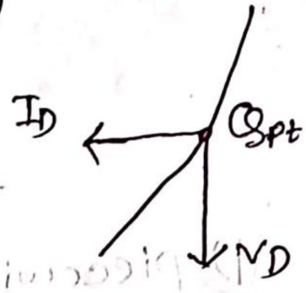
$V = RI$ or, $R = V/I$

এখানে, $R = V/I$, এবং Diode এর ক্ষেত্রে প্রতিটি point এর Resistance value সমান না। কিন্তু Coulomb law এর ক্ষেত্রে ওইগুলো সমান।

Type:-

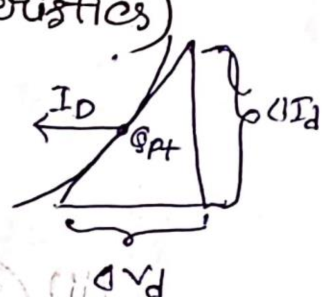
(নির্দিষ্ট voltage দেওয়া)

(i) DC or static, $R_D = \frac{V_D}{I_D}$



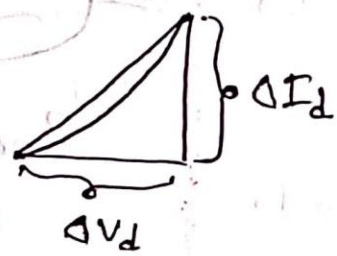
(Defined as a point on the characteristics)

(ii) AC or Dynamic, $r_d = \frac{\Delta V_d}{\Delta I_d} = \frac{26\,mV}{I_D}$



(Defined by a tangent line at the Q- point)

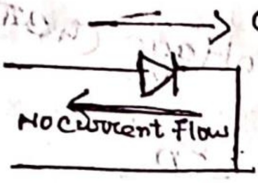
(iii) Avarage AC, $r_{av} = \frac{\Delta V_d}{\Delta I_d}\Big|_{pt.\ to\ pt.}$



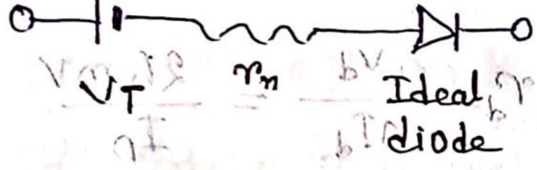
(Defined by a straight line between limits of operation).

[দুইটা পয়েন্টের voltage এর difference এবং current difference এর Ratio বের করতে হবে]

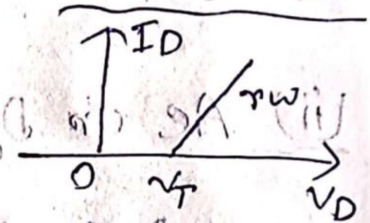
Diode equivalent circuit:-



(i) Piecewise-linear Model :-

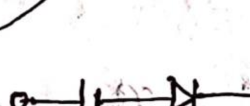


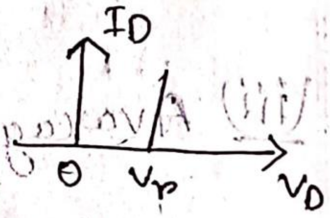
Characteristic



(ii) Simplified Mode : → (সবচেয়ে বেশি ব্যবহৃত)

Rnetwork ≫ r_{av}

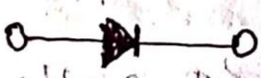


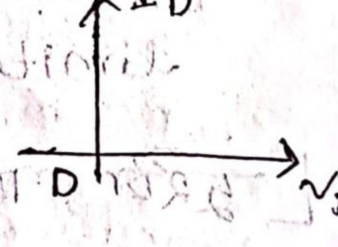


(iii) Ideal Device:-

Rnetwork ≫ r_{av}

Enetwork ≫ V_T





[সকল Diode 0.7v এর একটি বাধা কি Create করে এরপর যে সব current কেই Flow করে কোনো resistance ছাড়া।

◻ Transition & Diffusion capacitance :-

Forward Bias -এ voltage যেমন হবে Capacitance এর মান তত বাড়তে থাকবে।

~~আর রিভার্স বায়াস~~

At low frequencies and relatively small levels of capacitance the reactance of a capacitor, determined by $X_C = 1/2\pi f C$, is usually so high that it can be considered infinite in magnitude.

In the p-n semiconductor diode, there are two capacitive effects to be considered. Both types of capacitance are present in the forward & reverse bias regions. But one so outweighs (প্রভাবে অতিক্রম করা) the other in each region that we consider the effect ~~to be~~ of only one in each region.

Capacitance of a parallel plate capacitor is defined by, $C = \epsilon A/d$; where ϵ is the permitivity of the dielectric (insulator) between the plates of area A separated by a distance d. ~~ϵ is the permittivity of the dielectric (insulator)~~

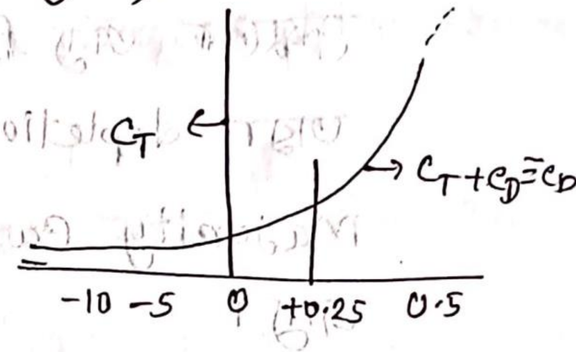
In a diode the depletion region behaves essentially like an insulator between the layers of opposite charge.

Since the depletion width (d) will increase with increased reversed-bias potential, the resulting transition capacitance will decrease.

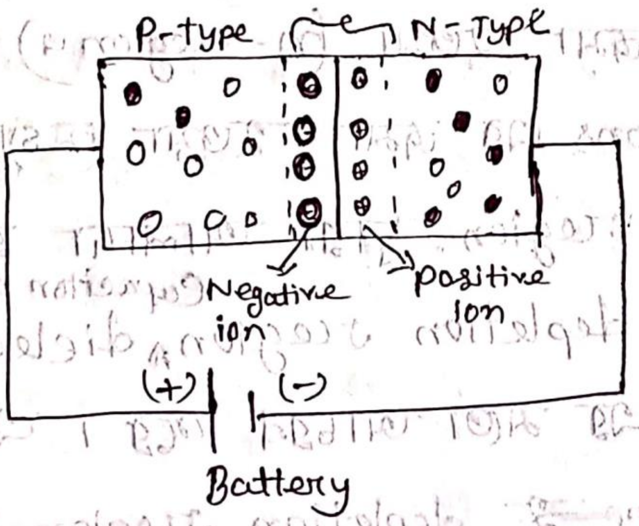
The capacitance is dependent on the applied reverse-bias potential has application in a number of electronic systems.

Transition (C_T), barriers, or depletion region Capacitance, is determined by,

$$C_T = \frac{C(0)}{\left(1+\left|V_R/V_K\right|\right)^n}$$



মূলকথা:-



(i) Depletion layer
(ii) Barrier potential
(iii) Diffusions Capacitances

Forward bias -এ voltage ~~দেওয়া হলে~~ . যদি p-n junction -এ দেওয়া হয় তবে ~~~~ electrons of n region will move to p-region & recombines with the holes. একই ভাবে, p-region এর holes n-region -এ move করবে। এর ফলে depletion region এর width কমে যায়। ~~elec~~ n-region হতে p-region -এ electrons গুলো minority হয়ে যায়

একইভাবে p-region এর holes n-region এ minority হয়ে যায়। অনেক গুলো charge carrier সেগুলো অন্য রিজিওনে যাওয়ার ট্রাই করছে তখন তারা depletion region-এ জমতে থাকবে। Majority carriers এর সাথে Recombined হওয়ার জন্য।

Holes এর জমা হওয়া (n-region এ) এবং p-region এ electrons এর জমা হওয়া সেগুলো পাতলা depletion region দ্বারা আলাদা হয়ে রয়েছে। আর এই depletion region Capacitor এর dielectric অথবা insulator এর মতো আচরন করে। এবং ~~উভয় পাশে Charge store হ~~ depletion region এর উভয় পাশে Charge store হতে থাকে সেগুলো Capacitor এর Conducting plates এর মতো আচরন করে থাকে।

যদি Diode এর মধ্য দিয়ে অনেক electric current Flow হয় তবে অনেক charge depletion region এ জমা হয়। এবং এর ফলে অনেক বড় diffusion capacitance ঘটে।

আর যদি ~~খুব~~ কম পরিমানে Current Flow হয় তবে ~~খুব~~ কম সংখ্যক charge depletion region এ জমা হয়। এর ফলে, small diffusion Capacitance ঘটে।।

যখন depletion region কমে যায় তখন diffusion Capacitance বৃদ্ধি পায়।।

The diffusion Capacitance value will be in the range of

Nano Farads (nF) to

Micro Farads (μF)।.

Formula:-

$$C_D = dQ/dV$$

C_D = Diffusion Capacitance

dQ = Change in number of minority Carriers stored outside the depletion region.

dV = Change in voltage applied across diode.

Impedence Infinity = open circuit

Light-Emitting Diodes (LED) :-

LED তে Gallium Arsenide phosphide (GaAsP) or gallium phosphide (GaP) ব্যবহার করা হয়।

The process of giving off light by applying an electrical source of energy is called electroluminescence.

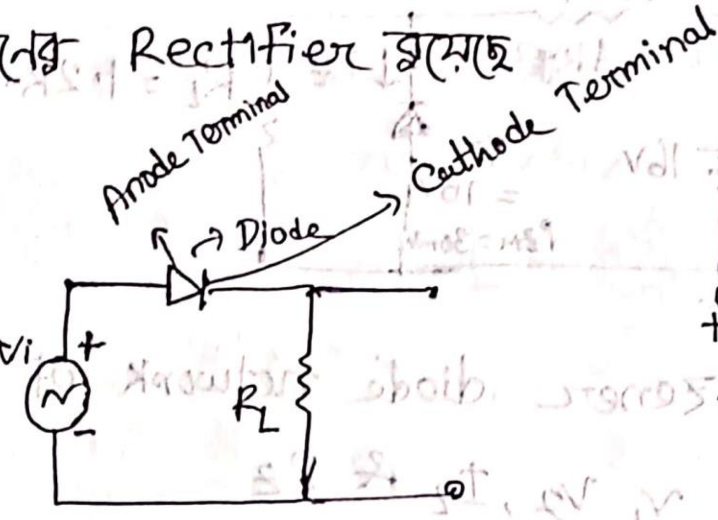
Math (How to solve diode Math)

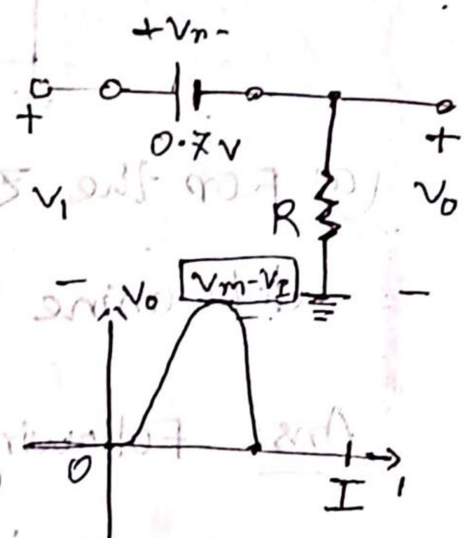
2.11 to 2.15 problem

2.7| Sinusoidal Inputs : Half-wave Rectification:-

AC হতে DC তে নেওয়ার কাজ করে Rectifier। বাংলায় বলে একমুখীকরণ।

2 ধরনের Rectifier রয়েছে

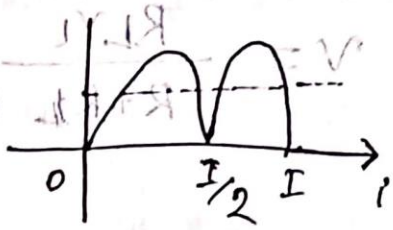




Half rectifier :-

Full-wave Rectifier:-

$V_{dc} \cong 0.636(V_m - 2V_p)$

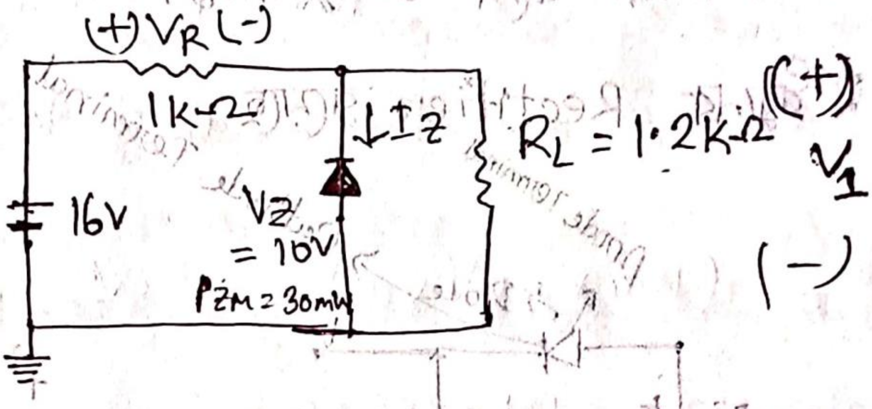


4. Zener Diodes:-

parallel Branch এ দুই রকম voltage হতে পারে না।

Math:-

(8)



(a) For the zener diode network of Fig 2.109 determine V_1, V_Z, I_Z & P_Z

Ans:- Following the suggested procedure the network is redrawn as shown in Fig 2.110 Applying Eq.(2.16) gives,

$$V = \frac{R_L V_1}{R + R_L} = \frac{1.2\,k\Omega(16V)}{1k\Omega + 1.2\,k\Omega} = 8.73V$$

(b) Repeat part (a) with $R_L = 3K\Omega$

Since $V = 8.73V$ & less than $V_Z = 10V$

So the diode is in OFF state; Substituting the open-circuit equivalent will result in the same network,

$V_L = V = 8.73V$ [In parallel Branch the voltage can't be different]

$V_R = V_i - V_L = (16V - 8.73V) = 7.27V$

$I_Z = 0A$

$P_Z = V_Z I_Z = V_Z(0A) = 0W$

(b) Here, $V = \frac{R_1 V_1}{R_1 + R_2} = \frac{3K\Omega \times 16V}{1K\Omega + 3K\Omega} = 12V$

$V = 12V$ is greater than $V_Z = 10V$. So the diode is on state.

$V_L = V_Z = 10V$

$V_R = V_i - V_L = (16V - 10V) = 6V$

$I_L = \frac{V_L}{R_L} = \frac{10}{3K\Omega} = 3.33 mA$

$I_R = \frac{V_R}{R} = \frac{6V}{1K\Omega} = 6\ mA$

$I_Z = I_R - I_L$

$= 6mA - 3.33mA$

$= 2.67\ mA$

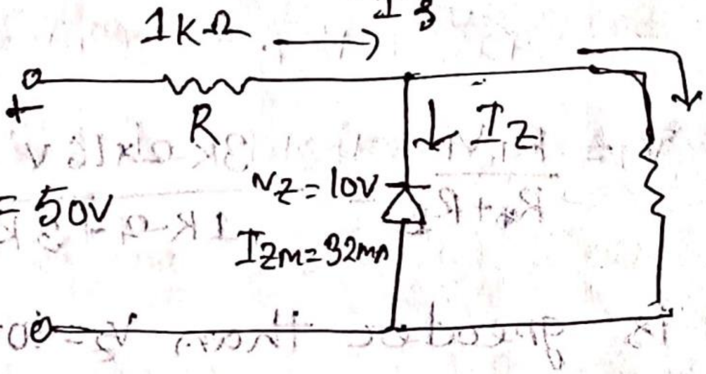
The power,

$P_Z = V_Z I_Z = (10V)(2.67\ mA)$

$= 26.7\ mW$

which is less than specified, $P_{ZM} = 30mW$

Math:-



(a) For the network of this figure, determine the range of R_L & I_L that will result in V_{RL} being maintained at 10V.

Solution:-

$$V_L = \frac{R_L}{R+R} V_i$$

~~$$or, 10 = \frac{R_L}{1k\Omega + R_L} 50$$~~

~~$$so, R_{Lmin} = \frac{1}{5} \cdot (1k\Omega + R_L)$$~~

$$V_{min} = \frac{(R_L + R)V_Z}{R_L} = \frac{(1200\Omega + 220\Omega)(20V)}{1200\Omega}$$

$$= 23.67V$$

$$I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L} = \frac{20V}{1.2k\Omega} = 16.67 \text{ mA}$$

$$I_{Rmin} = I_{ZM} + I_L = 60mA + 16.67 mA$$

$$= 76.67 mA$$

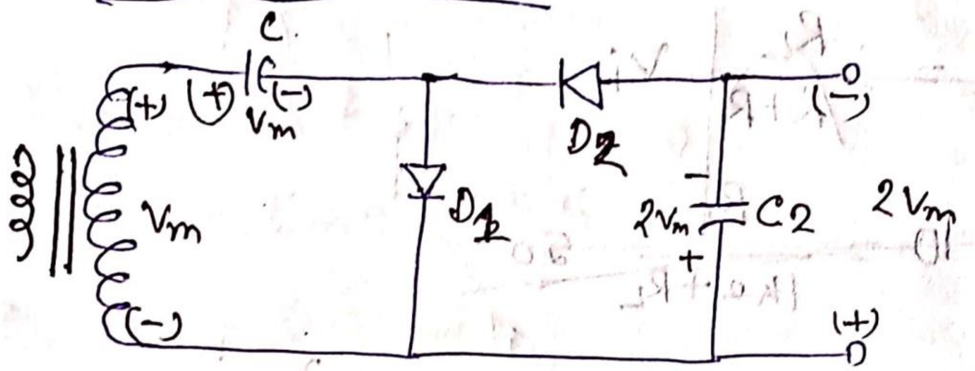
$$V_{imax} = I_{Rmax} R + V_Z$$

$$= (76.67 mA) \cdot (0.22k\Omega) + 20V$$

$$= 16.87 V + 20V$$

$$= 36.87 V.$$

Half wave voltage :-



Normal Bias এ D_1

Reverse Bias (+) হয় (−) এবং (−) হয় (+) সেক্ষেত্রে D_2

Ideal Diode (circuit explanation) :-

Forward Bias এ যে কাজ করে কিন্তু Reverse Bias এ কাজ করে না। এবং যার মাঝে 0.7 volt এর কোনো Drop নেই তাকেই Ideal Diode বলে।

☐ Simple series clippers (Ideal Diodes) :-

Signal এর একটা অংশকে ~~কেটে~~ কেটে ফেলা বাকি অংশকে অক্ষুন্ন রেখে এই জিনিসটা যে circuit এর মাধ্যমে আমরা achieve করি সে সার্কিটকে বলা হয় clipper circuit.।

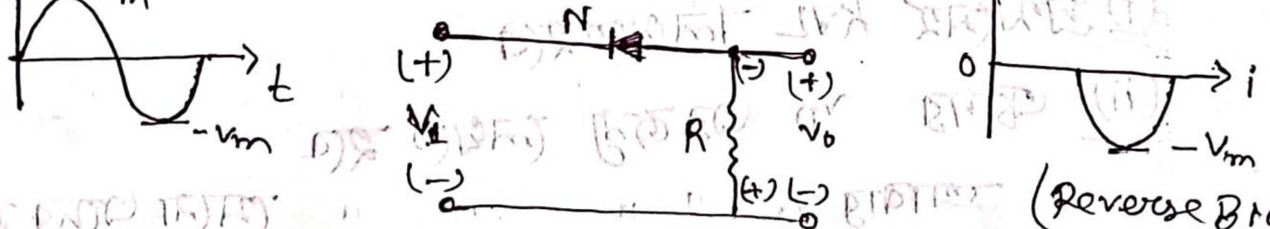
এখানে, চাইলে Negative/positive সাইড থেকে ~~কেটে~~ কেটে ফেলতে পারি। চাইলে বেশি কাটা যায় বা কম কাটা যায়।

Clipping of Signal :-

(i) Simple Series Clippers (এতে বাড়তি কোনো voltage থাকেনা)

প্রথমে positive & Negative half এ ভাগ করতে হবে

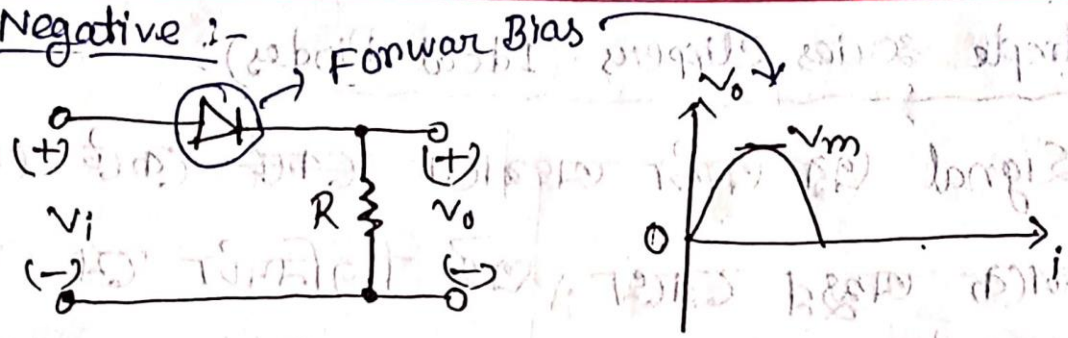
(Positive) Bias



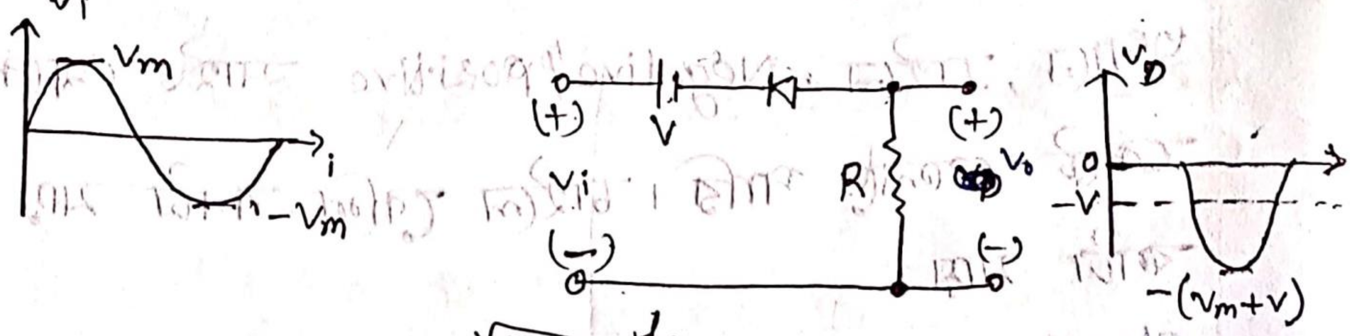
(Reverse Bias)

Forward Bias এ থাকলে v_0 থাকে, এবং কোনো Voltage Drop হয় না।

Negative :-



2| Biased Series Clipper :-



$$-V_i + V - V_D + V_0 = 0$$

$$V_D = -V_i + V + V_0 \quad\Big|\quad V_0 = V_i + V_D - V$$

$$V_D = -V_i + V$$

নিয়ম:-

(i) প্রথমেই KVL লিখতে হবে

(ii) এরপর V_D এর জন্য লেখতে হবে

আবার V_0 " " " " যেনো এদের মান বের করা যায়।

(iii) এরপর V_D এর জন্য লেখা equation এ V_0 কে ignore করতে হবে।

(মান positive হলে Forward, Negative হলে Reverse Bias)

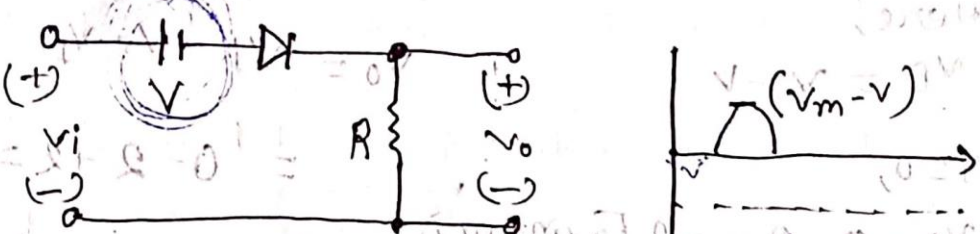
(iv) Diode Forward - Bias হলে V_o থাকবে

" " না " V_o " " না।

(v) মান বের করার জন্য,

( )

Negative:-



Calculations:-

$V_F = -1$

So, $V_D = -V_i + V = 1+2 = 3$

So, $V_o = V_i + V_D - V = -1+0-2 = -3$

(ii) $V_D = -V_i + V = 5+2$ ($V_i = -5$)

$= 7$

So, $V_o = V_i + V_D - V = -5+0-2 = -7$

(যত Negative মান বসানো হবে ততই বাড়বে)

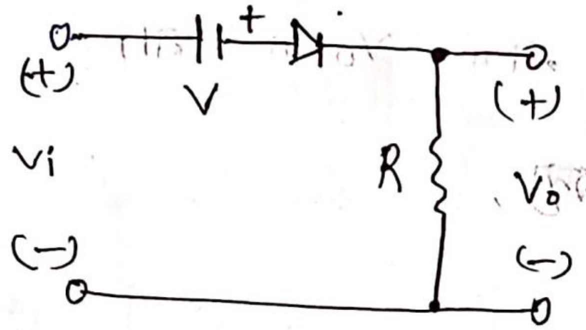
[V এবং Vi এর মাঝে পার্থক্য যত কম ধরা হবে ততই clip এর মাত্রা বেশি। (vice versa)]

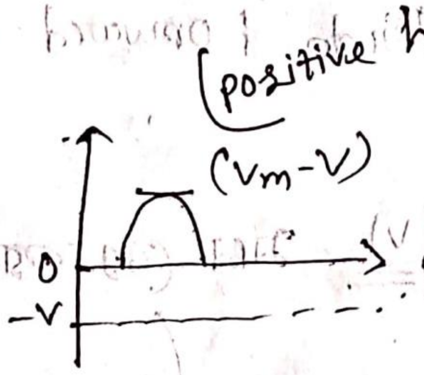
[এভাবেই Biasing voltage এর মাধ্যমে clip এর মাত্রাটা Control করাতে পারা যায়]

Forward Bias এ v_D এর মান 0 হয়।

Negative:-

(positive half cycle)





KVL,

$-V_i + V + V_D + V_0 = 0$

Here,

$V_D = V_i - V$

$V_0 = V_i - V - V_D$

$V_i = 0,$

$V_D = 0 - 2 = -2$ [V এর মান 2 ধরে]

(Reverse Bias)

$= 0 - 2 + 2 = 0$

$V_i = 1,$

$V_D = 1 - 2 = -1$

$V_0 = 1 - 2 + 1 = 0$

$V_i = 2,$

$V_D = 2 - 2 = 0$

$V_0 = 2 - 2 + 0 = 0$

$V_i = 3,$

$V_D = 3 - 2 = 1$

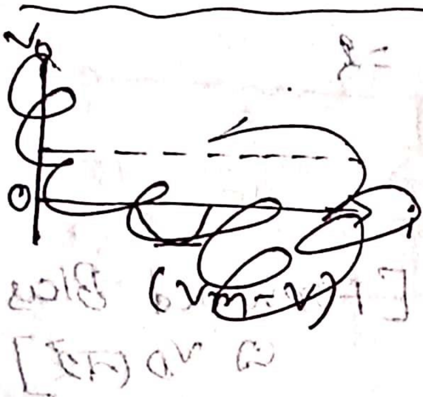
$V_0 = 3 - 2 - 0 = 1$ [Forward Bias এ $V_D = 0$]

$V_i = 5,$

$V_D = 5 - 2 = 3$

$V_0 = 5 - 2 - 0 = 3$

Negative half cycle



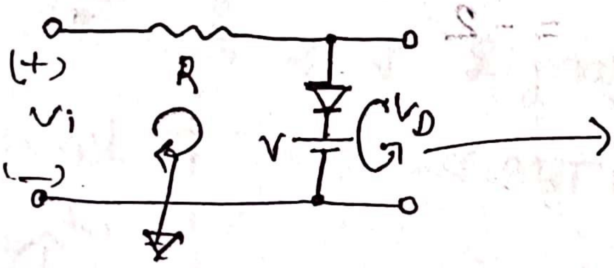
$V_D = V_i - V$
$= -5 - 2$
$= -7$

$V_0 = V_i - V - V_0$
$= -5 - 2 + 7$
$= 0$

~~Reverse~~ এ negative এ আর নেই]

practise:-

parallel clipper circuit



$-V_0 + V_D + V = 0$

Or, $V_0 = V_D + V$

$-V_i + V_R + V_D + V = 0$

$V_D = V_i - V_0$

Let, $V_i = 0$ & $V = 2$

So, $V_D = 0 - 2$
$= -2$

$V_i = 1$

$V_D = 1 - 2 = -1$

So,
$V_i = 0$ & $V = 2$

$V_0 = -2 + 2$
$= 0$

$V_i = 1$

$V_0 = -1 + 2$
$= 1$

$V_i = 2$

$V_D = 2 - 2$

$= 0$

$V_i = 3$

$V_D = 3 - 2$

$= 1$

$V_i = 2$

$V_o = 0 + 2 = 2$

$V_i = 3$

$V_o = 0 + 2$ [Forward Bias এ V_D নেই]

$= 2$

<u>Negative:-</u> $V_i = -1$

$V_D = V_i - V$

$= -1 - 2$

$= -3$

$V_i = -2$

$V_D = -2 - 2$

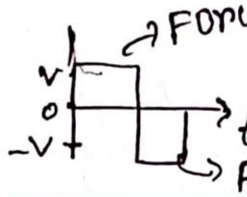
$= -4$

$V_o = -3 + 2$

$= -1$

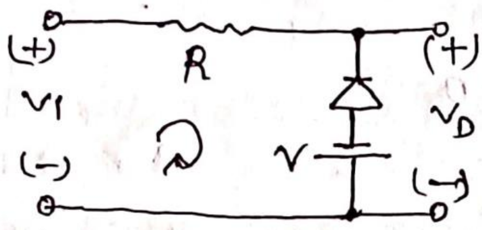
$V_o = -4 + 2$

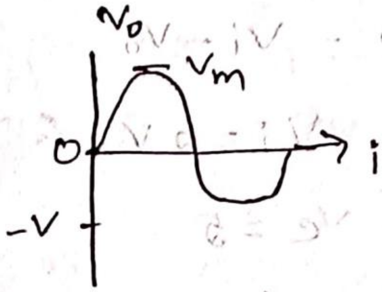
$= -2$



Clipper circuit
→ এর কাজ হলো Circuit এর একটা অংশ clip করা

Solve:-





$-V_i + V_R - V - V_D$

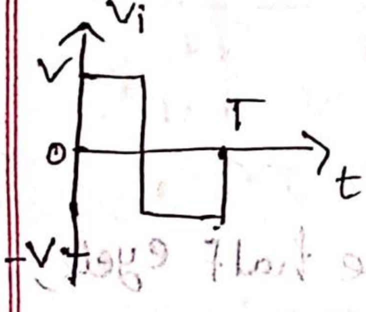
$V_D = -V_i \mp V$

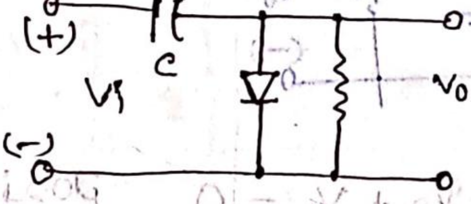
$V_o - V_D - V = 0$

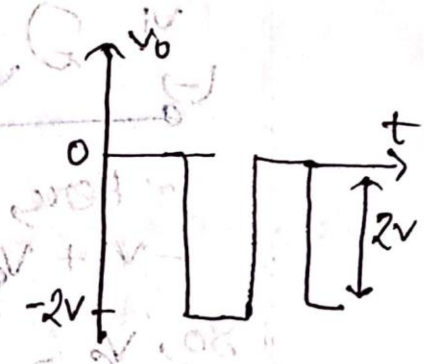
or, $V_o = V_D + V$

Clamper circuit

এর কাজ হলো Signal কে একটা Different DC level এ নিয়ে যাওয়া।







(Output)

so, ~~(positive ½ cycle)~~
$-V_i + V_C + V_o = 0$

Positive ½ cycle,

$V_C = V_i - V_o$

Let, $V_i = 5V$ & $V_o = 0$

So, $V_C = 5$

Negative ½ cycle,

$-V_i + V_C + V_o = 0$

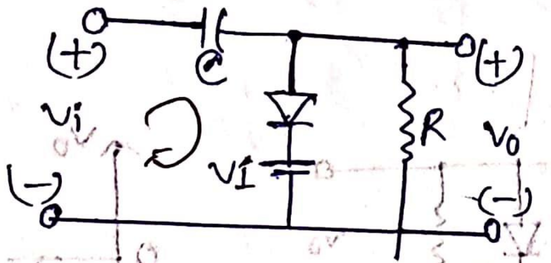
So, $V_o = +V_i - V_C$

Let, $V_i = -5V$,

So, $V_o = -5 - 5$

$= -10$ (২V বা দ্বিগুন হয়ে গেলো)

(২) With Biasing voltage:-



Here,

$-V_i + V_C + V_D + V_1 = 0$

So, $V_C = V_i - V_D - V_1$

$= 5 - 0 - 2$

$= 3V$

So, VC 3V Charge store হবে।

Positive half cycle,

Also,

$V_D = V_i - V_C - V_1$

$= V_i - V_1$

Let $V_i = 5V$, $V_1 = 2V$

So, $V_D = 5 - 2 = 3V$

Also,

$-V_0 + V_D + V_1 = 0$

So, $V_0 = V_D + V_1 = 0 + 2 = 2V$

Negative half cycle,

Let, $V_i = -5V$

$V_1 = 2V$

$V_D = V_i - V_C - V_1$

$= -5 - 3 - 2 = -10V$

So,

$V_C = V_i - V_D - V_1 = 5 - 0 - 2 = 3V$

Also,

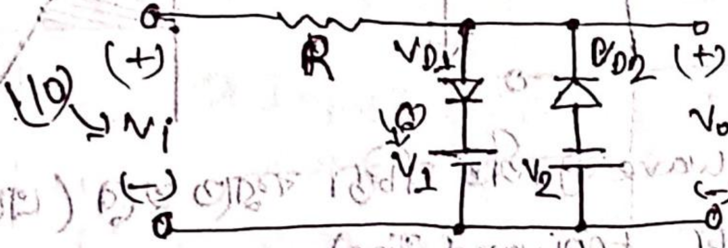
$-V_0 + V_D + V_1 = 0$

So, $V_0 = V_D + V_1$

$= -10V + 2$

$= -8V$

(10)



$-V_i + V_R + V_{D1} + V_1 = 0$

or, $V_{D1} = V_i - V_1$

$= 2 - 6$

$= -4$ (Reverse)

So, $V_0 = V_{D1} + V_1$

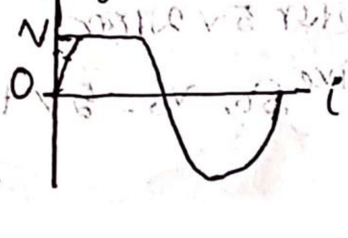
$= -4 + 6 = 2$

$-V_1 + V_R - V_{D2} - V_2 = 0$

$V_{D2} = -V_i + V_R - V_2$

$= -2 - 3 = -5$

(Reverse)



Clipper circuit

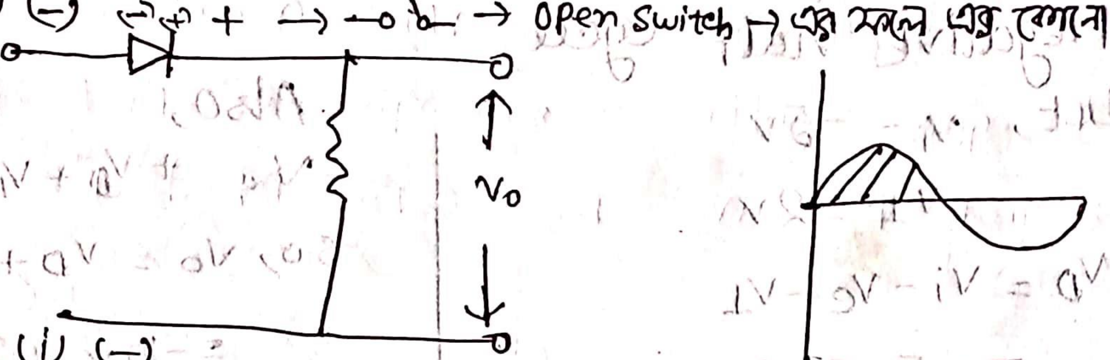
(Easy way to Remember) (School of Engineering)

=> কোনো Diode এ Anode (+) এবং Cathode(-) হলে তা Forward Bias হবে।

Anode এ wave থাকলে তাই হবে output.

(i) (+) (-) → o—o → close switch এ output পাবো।

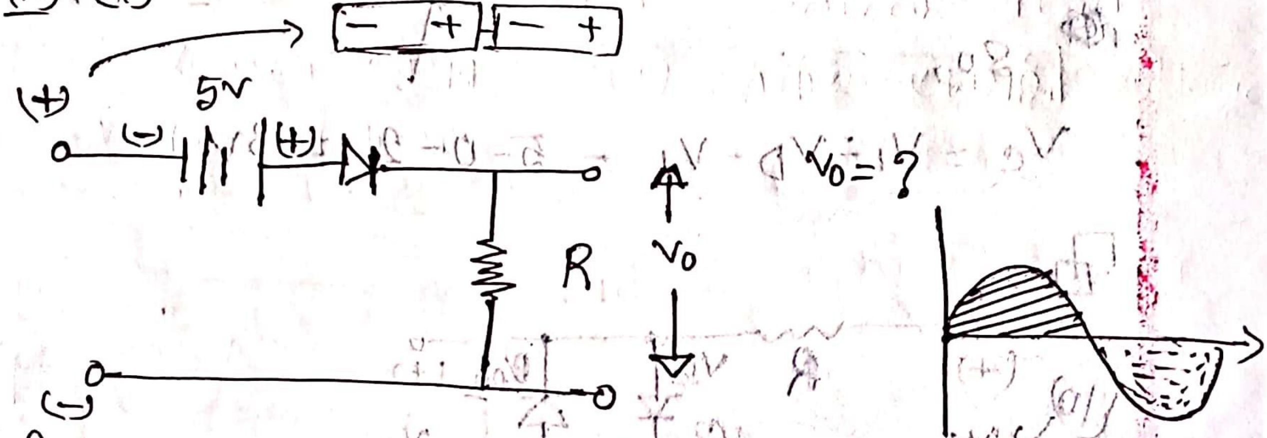
(ii) (-) (-)(+) + → —o o— → open switch → এর ফলে এর কোনো output হবে না



(i) (-)

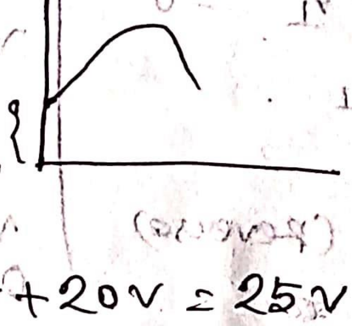
(ii) (+)

②



সমাধান।- ① প্রথমে wave ব্যতীত চিন্তা করতে হবে (এক্ষেত্রে Diode টা Forward Bias)

Output:-



0 হতে শুরু হয়নি কারণ Battery ছাড়া 5v থাকে

Positive So, $v_o = 5v + 20v = 25v$

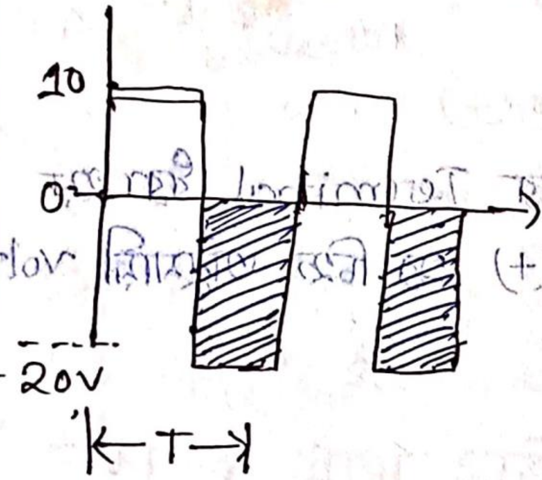
Negative: [+ -] [- +]

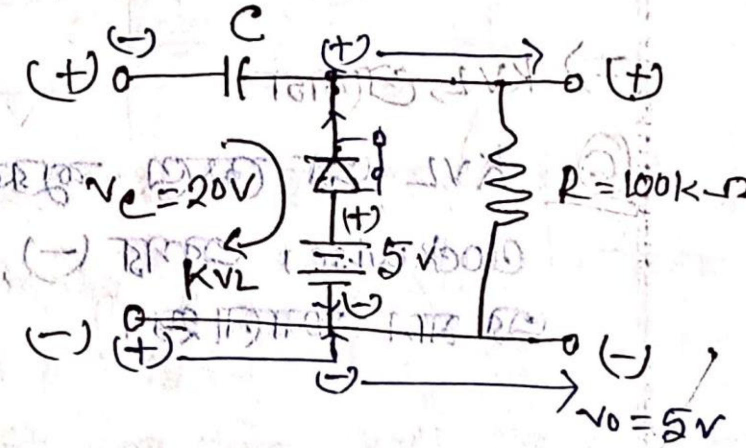
$= -20V + 5V$

$= -15V$

এখানে -5V পর্যন্ত Output পাবো। কারণ -5V, +5V কে vanish করাতে ব্যবহার করা হবে।

Clamper Circuit





কার্য:- ① Input এ কোন Cycle দিলে Diode Forward Bias।

(উক্ত চিত্রে উপরে (-) দিলে এবং নিচে (+) দিলে Forward Bias)

② শুরুতে (এই চিত্রে) Negative দিয়ে শুরু হবে

③ এখানে Diode এর ভিতর দিয়ে (-) এসে Output এ (-) হবে এবং (+) এসে output এ positive হবে।

④ আবার Capacitor এর (+), (−) নির্ধারণ করতে হলে শুরুতে যা থাকবে তা পুরো এক পাশে হবে। অপর

পাশে ভিন্নটি হবে। আর এটা Calculate করা হয় যে Condition দ্বারা solve করা হচ্ছে।

⑤ এরপর এই Capacitor এ voltage Drop হবে (V_c)। এটা নির্ণয় করতে হলে KVL লুপ চালাতে হয়।

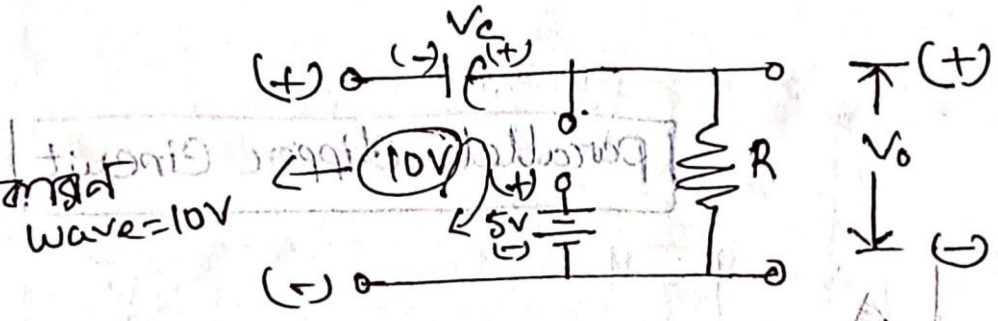
⇒ KVL প্রয়োগ

⑥ KVL এর ক্ষেত্রে, শুরুর Terminal ধরা হয় clockwise। এরপর (−), (+) এর চিহ্ন অনুযায়ী voltage এর মান বসানো হয়।

=> Solve :- Capacitor এর charging volt, KVL প্রয়োগ করে পাই,

$$+20 - V_c + 5V = 0$$

So, $V_c = 25V$



এখানে, যদি, positive দেওয়া হয় তবে Cathode হয় Positive এবং Anode হয় Negative। ফলে এটি open switch এ পরিণত হয়। এর ফলে আমাদের পুরো সার্কিটে লুপ দিয়ে KVL প্রয়োগ করতে হবে। (কারন open switch output পাওয়া যায় না।)

=> So, KVL প্রয়োগ করে পাই,

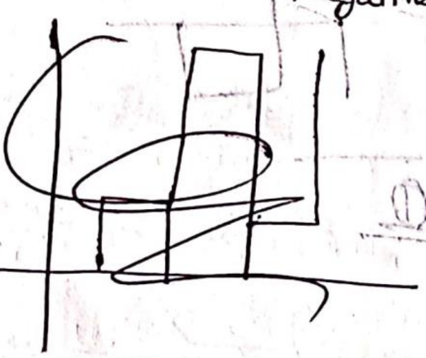
$$-10V - V_c + V_o = 0$$

So, $-10V - 25 + V_o = 0$

or, $-35V = -V_o$

So, $V_o = 35V$

So, Positive = 35V
Negative = 5V

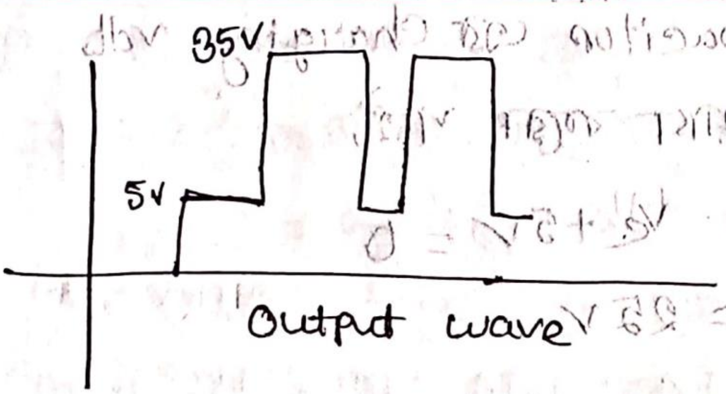


P.T.O

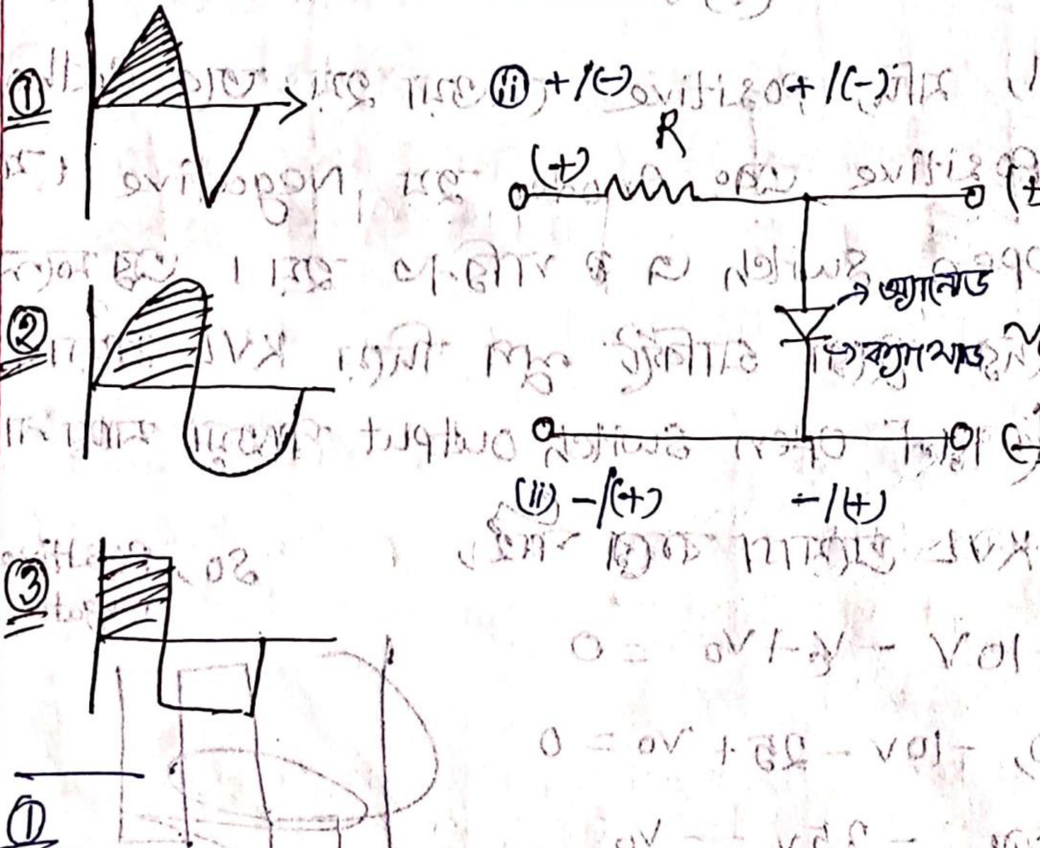
Diode এর ক্যাথোডে Negative

Anode এ positive হলে Diode হয় Forward Bias

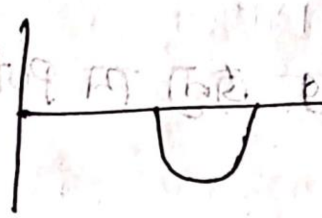
আবার, Cathode এ positive এবং Anode এ Negative হলে reverse bias (Open switch)



parallel clipper circuit

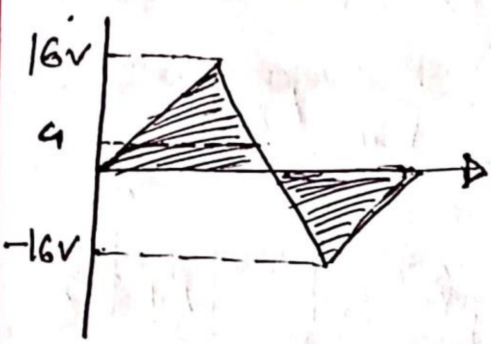


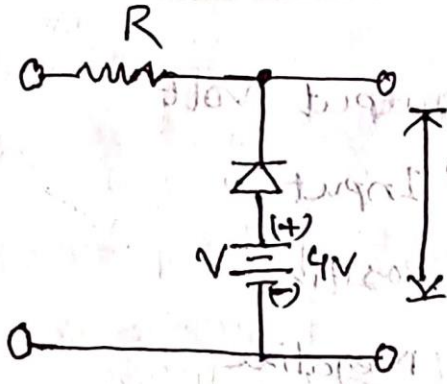
(2) Output



[কারন Forward Bias এ OFF switch হওয়ায় electron সুইচ এর ভিতর দিয়ে চলে যায়, Reverse Bias এ পারে না।]

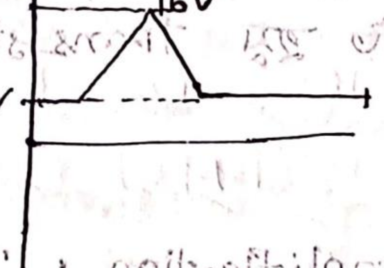
Math





$V_0 = ?$

Output:-

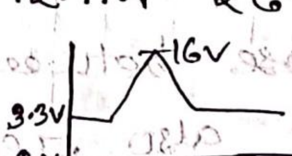


(i) Battery wave এবং Signal wave এক নয়।

সিলিকন Diode:—

$Si = 0.7V$ drop হবে। সেক্ষেত্রে Battery তে যত volt থাকবে তার থেকে মাইনাস হবে।

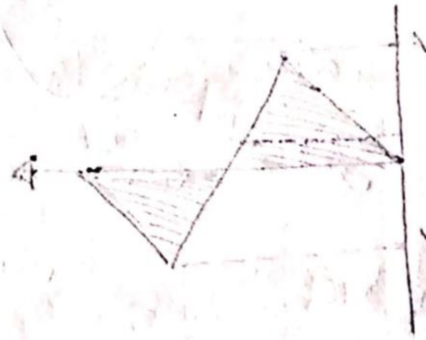
Output:-



Barrier Potential:-

p থেকে n এ
n " p তে যাওয়ার জন্য যে potential
এর সৃষ্টি হয়।

V_o = output volt
V_i = Input "
L = Positive
l = Negative



Transistor

৩টি টার্মিনাল নিয়ে গঠিত হয় transistor।

P-N-P , N-P-N ।

Transistor এর মূল কাজ Amplification ।

Amplification means increasing the signal strength.

- A transistor also acts as a switch to choose between available options.
- It also regulates the incoming current & voltage of the signal.

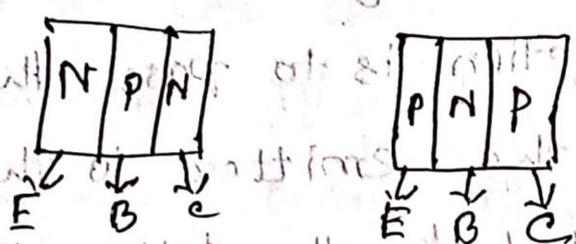
Construction:-

N-P-N or P-N-P

=> The transistor is a three terminal solidstate device which is formed by connecting two diodes back to back. Hence it has got two PN junctions.

=> This type of connection offers two types of transistors. They are PNP & NPN which means an N-type material between two p types and the other is a p-type material between two N-type respectively.

- The three terminals drawn from the transistor indicate Emitter, Base & collector terminals.



=> Construction of PNP & NPN Transistors

Emitter:-

- The left hand side of the shown structure can be understood as Emitter.
- This has a moderate size and is heavily doped as its main function is to supply a number of majority carriers, either electrons or holes.
- As this emits majority carriers, it is called as an Emitter.
- This is simply indicated with the letter E.

Base:-

- The middle material in the above Figure is the Base.
- This is thin & lightly doped.
- Its main Function is to pass the majority carriers from the emitter to the Collector.
- This is indicated by the letter B.

Collector :-

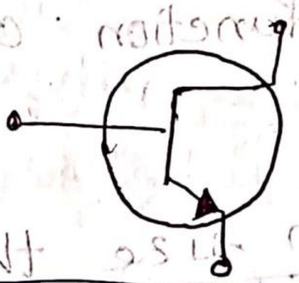
- The right-side material in the above Figure can be understood as a collector
- Its name implies its function of collecting the carriers.
- This is a bit larger in size than emitter and base. It is moderately doped.
- This is indicated by the letter c.

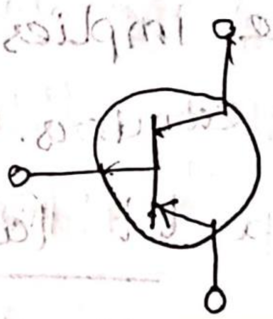
~~Symbols~~ :-

Symbol :-

- The arrow-head in the figures indicated are the emitter of a transistor.
- Due to the specific functions of emitter & collector, they are not interchangeable. Hence the terminals are always to be kept in mind while using a transistor.
- In a practical transistor, there is a notch

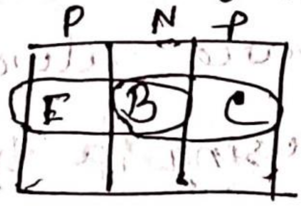
present near the emitter lead for identification. The PNP & NPN transistors can also be differentiated using a Multimeter.


Symbol of NPN transistor


Symbol of PNP transistor

Transistor Biasing:-

As we know that a transistor is a Combination of two diodes, we have two junctions here. As one junction is between the emitter & base, that is called as Emitter-Base junction & likewise, the other is Collector-Base junction.



• (Biasing is controlling the operation of the circuit by providing power supply.) The function of both the PN junctions is controlled by providing bias to the circuit through some DC supply.

- Emitter-Base junction কে অবশ্যই Forward Bias হতে হবে।
- Collector-Base junction কে অবশ্যই Reverse Bias হতে হবে।

• In P-N-P junction,

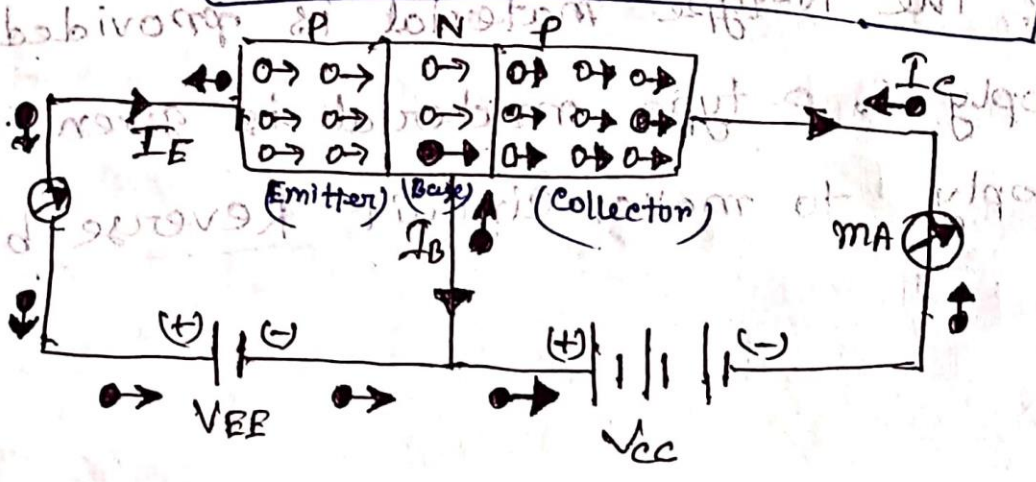
- The N-type material is provided negative supply & P-type material is given positive supply to make the circuit Forward bias.
- The N-type material is provided positive supply & P-type material is given negative supply to make circuit Reverse bias.

⊕ By Applying the power, the emitter-Base junction is always Forward biased as the emitter resistance is very small. The collector base junction is reverse biased, and its resistance is a bit higher. Therefore, it is called Transistor [Transfer of Resistance].

Conventional current :-

The direction of current indicated in the circuits above, also called as the conventional current, is the movement of hole current which is opposite to the electron current.

Operation of PNP Transistor



- The voltage V_{EE} provides a positive potential at the emitter which repels (তাড়াইয়া দেয়া) the holes in the P-type material & these holes cross emitter-base junction, to reach the base region.
- There a very low percent of holes recombine with free electrons of N-region. This provides very low current which constitutes the base current I_B.
- The remaining holes cross the collector-base junction, to constitute collector current I_C, which is the hole current.

Hence, we can understand that,

- The conduction in PNP transistor takes place through holes.
- The collector is slightly less than the emitter current.
- The increase or decrease in the emitter current affects the collector current.

- The voltage V_{EE} provides a positive potential at the emitter which repels (প্রত্যাখ্যান করা) the holes in the P-type material & these holes cross emitter - base junction, to reach the base region.
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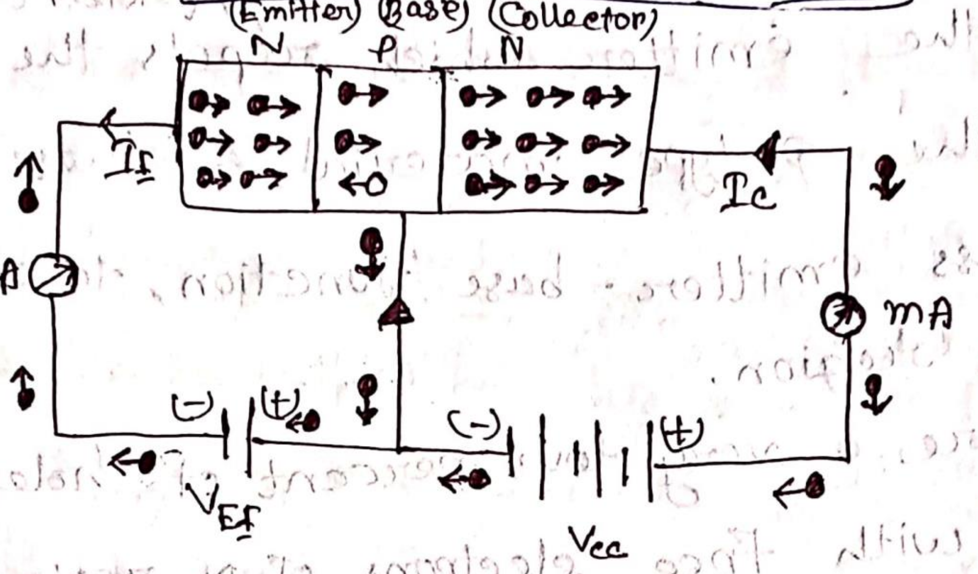
Operation NPN Transistor



⇒ The voltage V_{EE} provides a negative potential at the emitter which repels the electrons in the N-type material and these electrons cross the emitter-base junction, to reach the base region.

⇒ There a very low percent of electrons recombine with free holes of p-region. This provides very low current the base current I_B,

⇒ The remaining ~~holes~~ electrons cross the collector-base junction, to constitute the collector current I_C.

Hence we can understand that -

(i) The conduction in a NPN transistor takes place through electrons.

(ii) The collector current is ~~highter~~ higher than the emitter current.

(iii) The increase or decrease in the emitter current affects the collector current.

Advantages of Transistor

1) High voltage gain.

2) Lower supply voltage is sufficient.

3) Most suitable for low power applications.

4) Smaller & lighter in weight.

5) Mechanically stronger than vacuum tubes.

6) No external heating required like vacuum tubes.

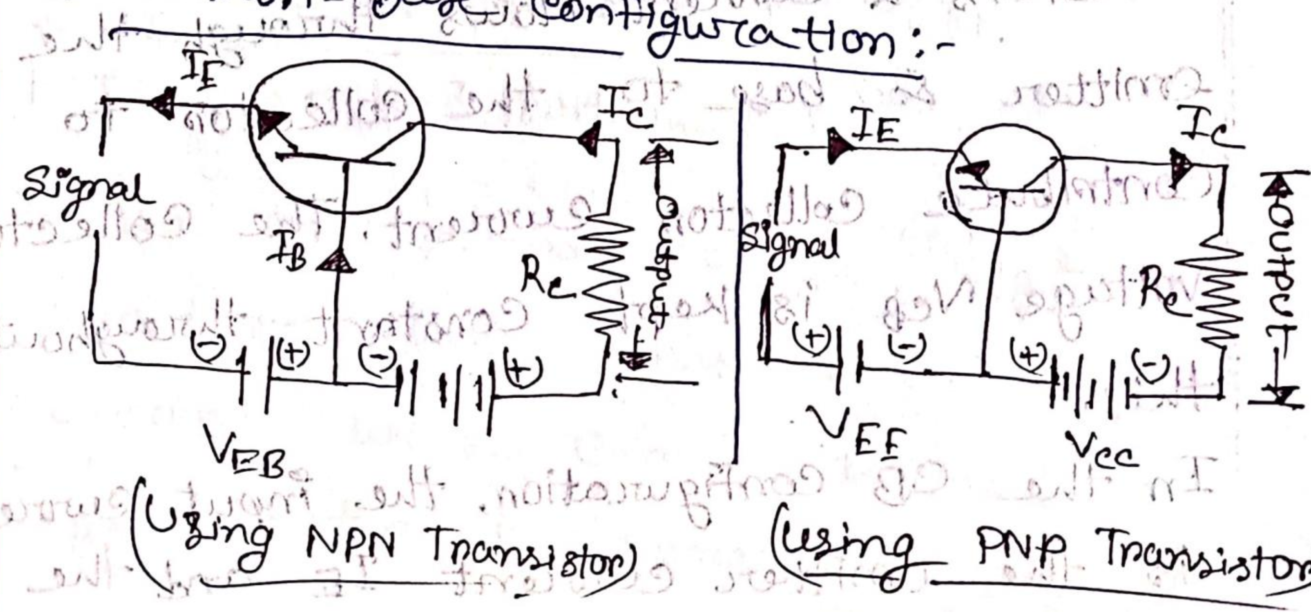
7) Very suitable to integrate with resistors & diodes to produce ICs.

Configurations Of Transistor

Transistor has 3 terminals. The emitter, the base & the Collector. Using these 3 terminals the transistor can be connected in a circuit with one terminal common to both input & Output in a three different possible configurations.

The three types of configurations are Common Base, Common Emitter, Common Collector Configurations. In every configuration the emitter Junction forward biased & the Collector Junction is reversed biased.

(1) Common - Base Configuration:-



$\frac{Output}{Input} > 1$ = Amplification

$\Rightarrow \frac{V_o}{V_i} \Rightarrow \frac{I_o}{I_i} \Rightarrow \frac{P_o}{P_i} \Rightarrow \frac{I_C}{I_E}$

I_E (সবচেয়ে বড় current) $= I_B + I_C$

$I_C < I_E$ That means $\frac{I_C}{I_E} < 1$

⇒ Common Base Configuration এর ক্ষেত্রে Current এর কোনো Amplification সম্ভব না।

এর মানে হলো ~~Current Bo~~ Common Base Configuration এর ক্ষেত্রে কোনো Amplification সম্ভব না।

⇒ In NPN transistor in CB configuration, when the emitter voltage is applied, as it is forward biased, the electrons from the negative terminal repel the emitter electrons & current flows through the emitter & base to the collector to contribute collector current. The collector voltage V_{CB} is kept constant throughout this.

In the CB configuration, the input current is the emitter current I_E and the output current is the collector current I_c.

Current Amplification Factor α:-

The ratio of change in collector current ΔI_c to the change in emitter current ΔI_E when the ration of change in collector current ΔI_c to the change in emitter current ΔI_E when collector voltage V_{CB} is kept constant, is called as current amplification factor. It is denoted by α

$$\alpha = \frac{\Delta I_c}{\Delta I_E} \text{ at constant } V_{CB}$$

Total collector current:-

$$I_c = \alpha I_E + I_{leakage}$$

If the emitter-base voltage $V_{EB} = 0$, even then, there flows a small leakage current, which can be termed as I_{CBO} collector-base current with output open

The collector current therefore can be expressed as-

$I_C = \alpha I_E + I_{CBO}$

We know,

$I_E = I_C + I_B$ —— (i)

$I_C = \alpha (I_C + I_B) + I_{CBO}$ —— (i) বসিয়ে)

$I_C (1 - \alpha) = \alpha I_B + I_{CBO}$

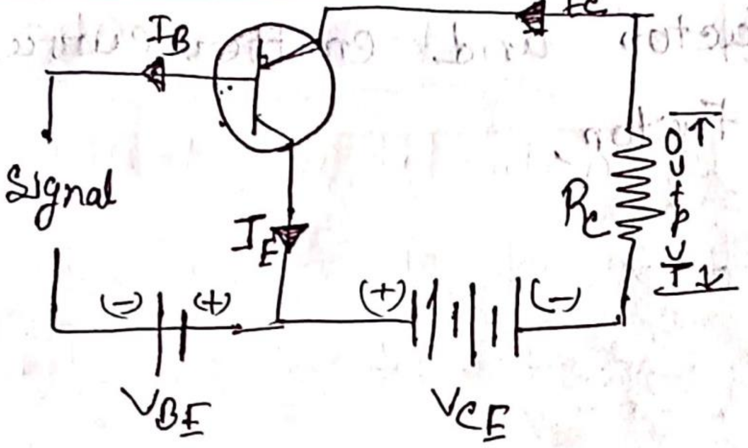
$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{I_{CBO}}{1-\alpha}\right)$

$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO}$

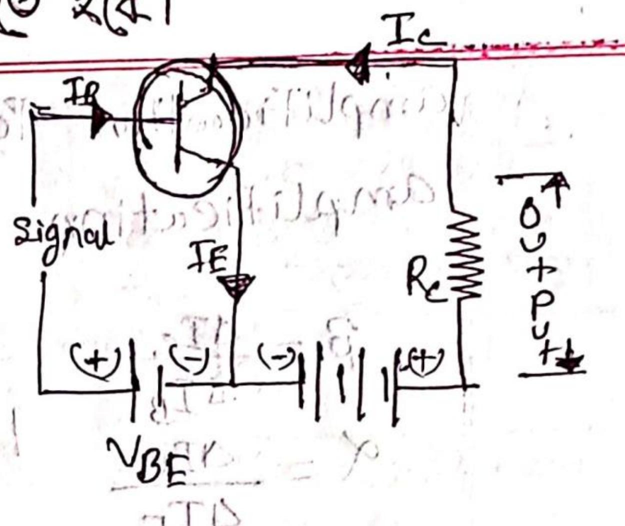
Common Emitter (CE) Configuration :-

PNP → Forward Bias হতে হলে P (+) ও N (−) এর সাথে যুক্ত রাখতে হবে।

যে কোনো Configuration এর ক্ষেত্রেই Emitter কে Forward Bias -এ রাখতে হবে।



(Using PNP Transistor)



(Using NPN Transistor)

⇒ The emitter junction is forward bias & Collector junction is reversed biased. The flow of electrons is controlled in the same manner. The input current is the base current I_B and the output current is the collector current I_C here.

Base current Amplification Factor (β)

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

Relation between β & α:-

Let us derive the relation between base current amplification factor and emitter current amplification factor,

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

* $I_E = I_B + I_C$

$$\Delta I_E = \Delta I_B + \Delta I_C$$

$$\Delta I_B = \Delta I_E - \Delta I_C$$

$$\beta = \frac{\Delta I_C}{\Delta I_E - \Delta I_C} = \frac{\frac{\Delta I_C}{\Delta I_E}}{\frac{\Delta I_E}{\Delta I_E} - \frac{\Delta I_C}{\Delta I_E}}$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

* $I_C = \beta I_B + I_{CBO}$

Fixed-Biased Circuit বোঝার উপায়!-

Emitter Terminal এ কোনো Resistance লাগানো থাকবে না।

Fixed-Bias Circuit:-

এক্ষেত্রে AC Signal কে Ignore করে শুধু Fixed-Bias Circuit ও হিসেব করা যায়।

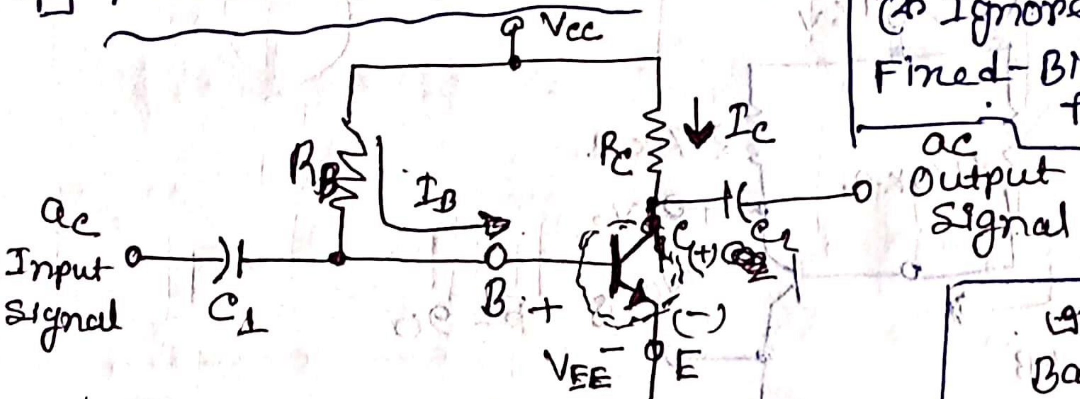


Figure:- Fixed-Bias Circuit

এর একটি অংশ Base terminal এর সাথে, আরেকটি যুক্ত করা হয় Resistance এর মাধ্যমে একে বলা হয় Base Resistance আরেকটি terminal কে Resistance Rc এর মাধ্যমে Collector Terminal এর সাথে যুক্ত করা হয়। একে বলে Collector Resistance

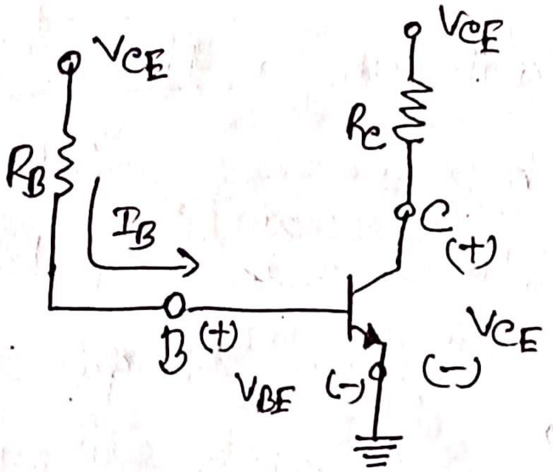


Figure:- dc equivalent of

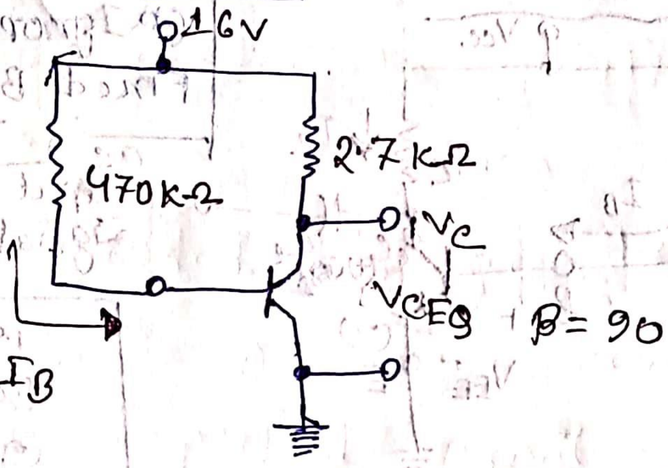
=> Solve:-

প্রথমে I_B বের করা (Base terminal Flow হওয়া current)

=> I_B বের করার জন্য Input side মান ব্যবহার করাতে হবে।

=> V_C বের করার জন্য Output side এর মান ব্যবহার করতে হবে।

Math



Determine :-

(i) I_{BQ}

(ii) I_{CQ}

(iii) V_{CEQ}

(iv) V_{BE}

(iv) $V_{BE} = V_B - V_E = V_B - 0$

$= V_B = 0.7\,V$

Steps

- ✱ প্রথম কাজ হলো I_B বের করা।
- ✱ এরপর $I_c = \beta I_B$ বের করা।
- ✱ V_{CE} বের করা I_c হতে।

Base Emitter → Forward Bias এ থাকতে হবে।

Collector Base → Reverse Bias এ থাকতে হবে।

All Formulas

$V_{CE} + I_C R_C - V_{CC} = 0$

or, $V_{CE} = V_{CC} - I_C R_C$ ——— ①

$V_{CE} = V_C - V_E$ ——— ②

$V_{CE} = V_C$ ——— ③

$V_{BE} = V_B - V_E$ ——— ④

$V_{BE} = V_B$ ——— ⑤

এখানে,

$V_E = 0$ হবে

Transistor Saturation

The term saturation is applied to any system where levels have reached their maximum values. A ~~sto~~ saturated sponge is one that cannot hold another drop of liquid. For a transistor operating in the ~~stu~~ saturation region. The current is a maximum value for the particular design. Change the design & the corresponding saturation level may rise or drop. Of course, the highest saturation level

V.

is defined by the maximum collector current as provided by the specific sheet.

~~St~~ Saturation conditions are normally avoided because the base-collector junction is no longer reverse-biased and the output amplified signal will be distorted.

$$V_{CE} = V_{CC} - I_C R_C$$

we call it saturation when,

$V_{CE} \leq 0.3V$ [অর্থাৎ এই সময়ে transistor টা ~~St~~ Saturation region এ প্রবেশ করে]

$V_{CB} = V_{CE} - V_{BE}$
মতান্তরে, $V_C - V_B$ 〉 মান (+) হতে হবে।

V_{CE} কে 0 ধরে Math করা হয়, কারণ 0.3 এবং 0 এর মাঝে তেমন কোনো পার্থক্য নেই।

Transistor Biasing:

Transistor Biasing এর দুইটি উদ্দেশ্য :

(i) To set an operating-point.

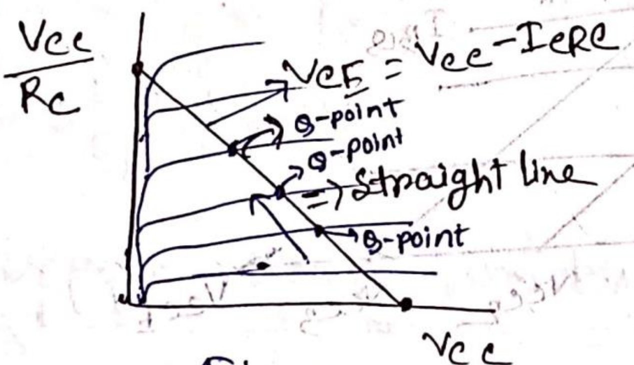
(ii) To ensure temperature stability.

We Know that,

$$I_C = \beta I_B + I_{CEO}$$

Fixed

Load-Line Analysis:-



$V_{CE} = 0$

$I_C = \frac{V_{CC}}{R_C}$

$I_C = 0$

$V_{CE} = V_{CC}$

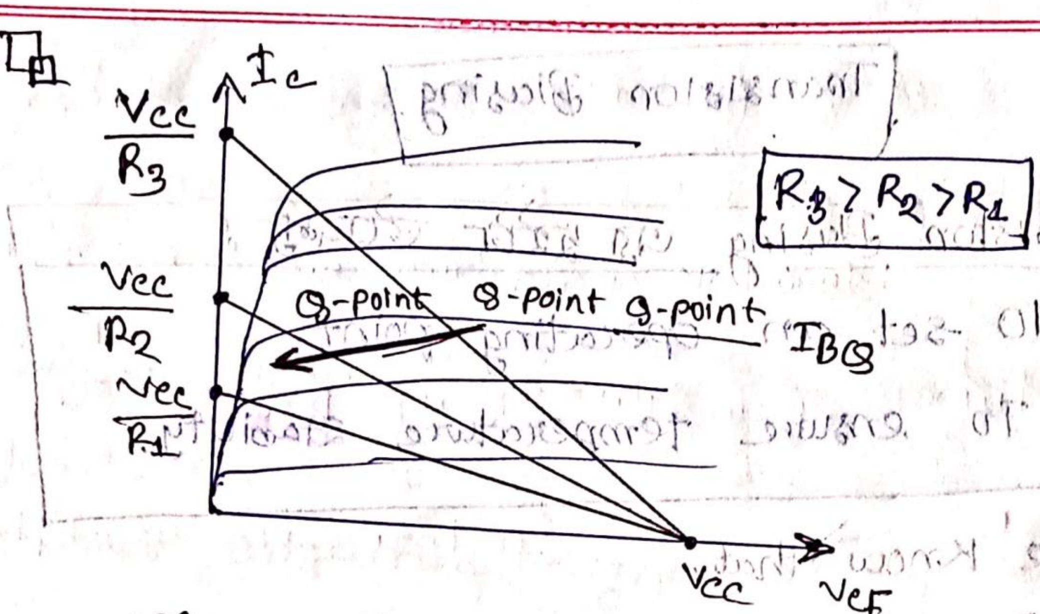
Fig: Movement Q-point with increasing levels of I_B

$V_{CE} = V_{CC} - I_C R_C$ is similar to a straight line eqn

$$y = mx + c$$

or $V_{CE} = -R_C I_C + V_{CC}$

The straight line in the Figure is Known as Load-Line.



এখানে R_c বাড়ানো-কমানোর মাধ্যমে operating point ~~Load-line~~ এ পরিবর্তন করা সম্ভব।

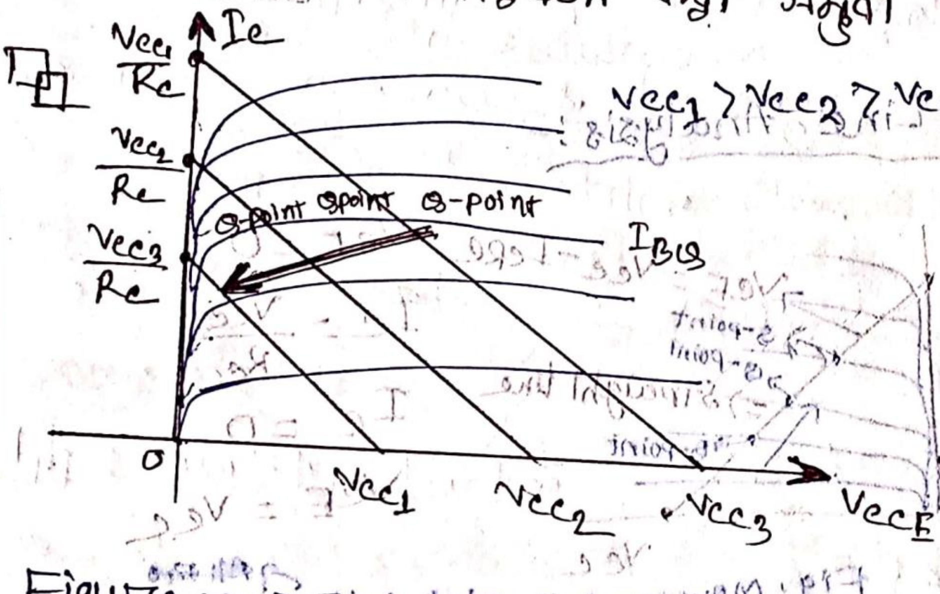


Figure:- Effect of lower values of V_{CC} on the Load line & Q-point

এখানে V_{CC} এর মান বাড়ানো - কমানোর মাধ্যমে operating point এর পরিবর্তন হয়।

Fixed Bias Design

VBC দিয়ে Reverse Bias test হয়

Fixed Bias এর ডিজাইনিং এর ক্ষেত্রে, V_{CC}, R_B ও R_C বের করতে হয়

Emitter-Stablized Bias Circuit:-

Note:-

(i) $V_{AB} = V_A - V_B$ [অর্থাৎ VA point VB point হতে কি পরিমাণ potential এ আছে]

(ii) $V_A = V_A - V_0$ [অর্থাৎ, VA point Ground potential হতে কি অবস্থায় আছে।

Emitter Bias circuit এর ক্ষেত্রে ~~Stabi~~ temperature stability বৃদ্ধি পায়।

4.5] Voltage Divider Bias circuit:-

4.6] DC BIAS with Voltage Feedback:-

4.7] Miscellaneous Bias Configuration:-

(page-174)

⊛ Biasing circuit:-

⊞ Transistor Switching Network:-

ট্রানজিস্টর দিয়ে switching circuit তৈরি।

⊞ Bias Stabilization:-

The stability of a system is a measure of the sensitivity of a network to variations in its parameters. In any amplifier employing a transistor the collector current I_c is sensitive to each of the following parameters.

⇨ If its output is under control then it's system is stable

⊞ Stability Factors, $S(I_{co})$, $S(V_{BE})$ and $S(\beta)$:-

$$S(I_{co}) = \frac{\Delta I_c}{\Delta I_{co}} \quad \text{——— (1)} \rightarrow \text{Reverse situration current}$$

$$S(V_{BE}) = \frac{\Delta I_c}{\partial V_{BE}} \quad \text{——— (2)} \rightarrow \text{Base-Emitter voltage}$$

$$S(\beta) = \frac{\Delta I_c}{\Delta \beta} \quad \text{——— (3)} \rightarrow \text{Current Amplification Factor}$$

যেখানে I_c এর মান নিয়ন্ত্রণে।

The higher the stability factor, the more sensitive the network to variations in that parameter.

$S(I_{co})$:- [Emitter Bias Configuration]

$$S(I_{co}) = (\beta+1) \cdot \frac{1 + R_B/R_E}{(\beta+1) + R_B/R_E} \quad (4.54)$$

For $(R_B/R_E) \gg (\beta+1)$ will reduce to the following,

$$S(I_{co}) = \beta + 1 \quad (4.55)$$

RB হতে RE এর মান বাড়ালে স্ট্যাবিলিটি ভালো হবে।

Feedback – Bias Configuration → (কোয়েক পাতায় হাইলাইট লেখা আছে)

Physical Impact:-

~~Equation~~ $\left(I_B = \frac{V_{CC} - V_{BE}}{R_B} \right)$

[Equations of the type developed above often fail to provide a physical sense for why the networks perform as they do]

with the collector current determined by,

$$I_C = \beta I_B + (\beta + 1) I_{co} \quad (4.61)$$

Chapter - 05

Field Effect Transistors (FET)

⊛ BJT ও FET:- (পার্থক্য)

BJT:- এটি একটি Current Control Device.

FET:- এটি একটি voltage Control Device.

⊛ BJT transistor is a bipolar device, কারণ hole ও electron উভয়ই Current Conduction এ অংশগ্রহণ করে।

FET is a unipolar device depending solely on either electron (n-channel) or hole (P-channel) conduction.

⊛ FET is high input impedance. At level of 1 to several hundred megohms it far exceeds the typical input resistance levels of the BJT transistor configurations.. a very important characteristic in the design of

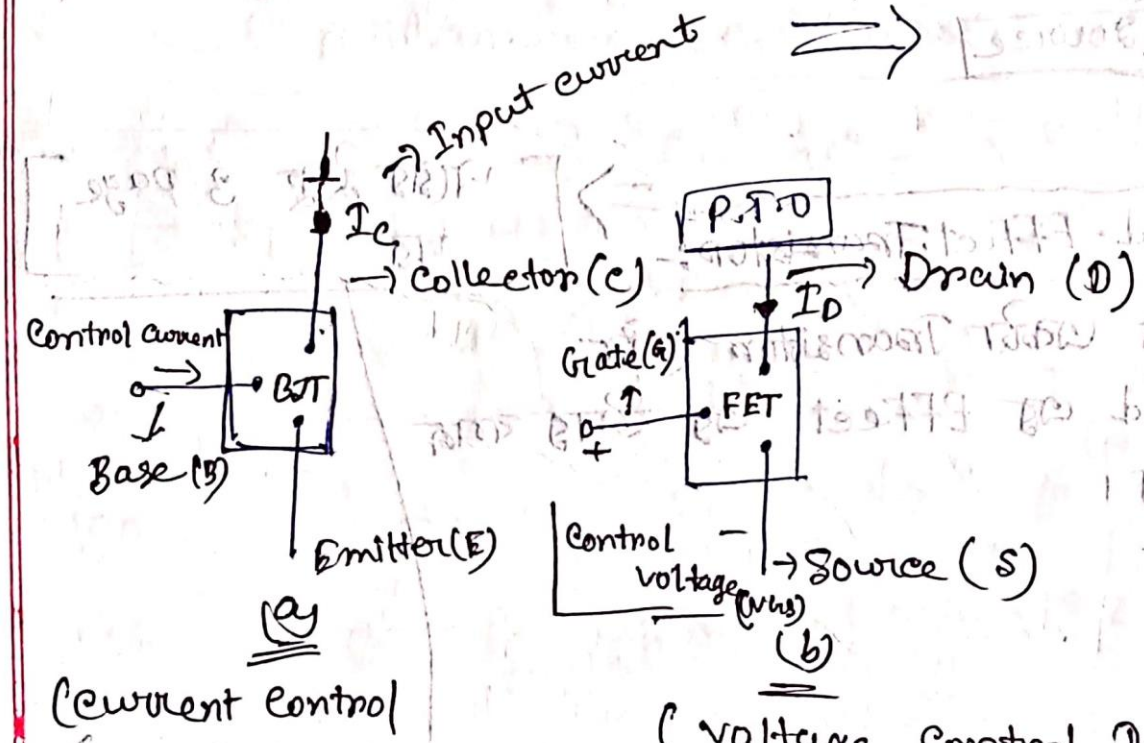
⊛ FET খুব ছোট করে বানানো যায়। এটাকে Integrated Circuit (IC) হিসেবে তৈরি করা যায়।

There are two types of FETs ~~will be introduced in this chapter~~.

1) The Junction Field-Effect Transistor (JFET)

2) The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET).

The MOSFET category is further broken down into depletion and enhancement types.



(current control Device)

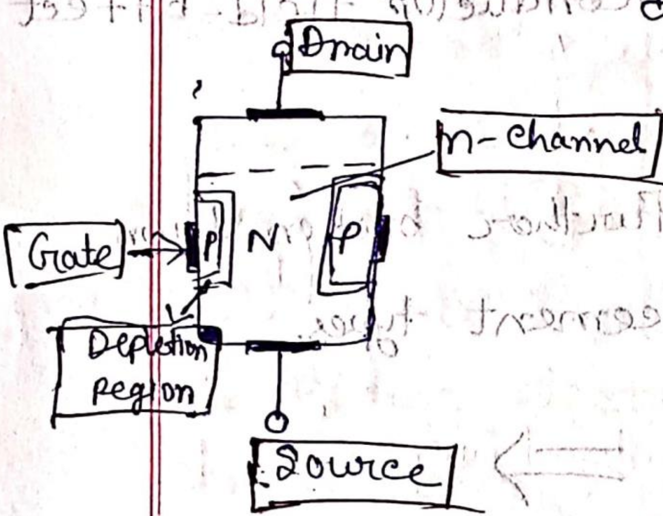
(voltage control Device)

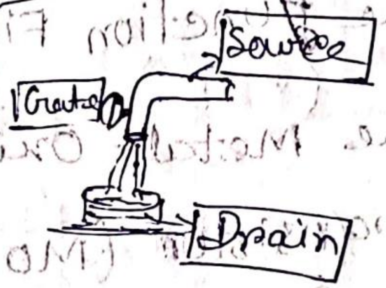
JFET :-

Amitter —— Source

Base —— Gate

Collector —— Drain





Field-Effect Transistor :- → [পাশের টুকু 3 page চার]

এমন একটা Transistor যেটা Field এর Effect এর উপর কাজ করে।

Chapter-5

~~Field Effect Transistors.~~

4.12) Bias Stabilization:-

The stability of a system is a measure of the sensitivity of a network to variations in its parameters.
In any amplifier employing a transistor the collector current I_c is sensitive to each of the following parameters.

Variation of Silicon Transistor parameters with Temperature

$T(^\circ C)$	$I_{CO}(nA)$	β	$V_{BE}(V)$
-65	0.2×10^{-3}	20	0.85
25	0.1	50	0.65
100	20	80	0.48
175	3.3×10^{3}	120	0.3

Operating point ও Temperature এর সাথে পরিবর্তন হয়।

Stability Factors, $S(I_{CO})$, $S(V_{BE})$, and $S(\beta)$:-

$$S(I_{CO}) = \frac{\Delta I_C}{\Delta I_{CO}} \quad (4.51)$$

$$S(V_{BE}) = \frac{\Delta I_C}{\Delta V_{BE}} \quad (4.52)$$

$$S(\beta) = \frac{\Delta I_C}{\Delta \beta} \quad (4.53)$$

[Stability Factor এর মান যতটুকু সম্ভব কম করতে হবে]

Note:-

For a particular configuration, if a change in I_{CO} fails to produce a significant change in I_C, the stability factor defined by $S(I_{CO}) = \Delta I_C / \Delta I_{CO}$ will be quite small.

Network that are quite stable and relatively insensitive to temperature variations have low stability factors.

Voltage Divider Bias :-

$$S(I_{CO}) = (\beta+1)\frac{1+R_{Th}/R_E}{(\beta+1)+(R_{Th}/R_E)}$$

R_E এর মান R_{Th} এর থেকে বেশি রাখলে হবে

9 → 18 → 90
8 → 16 → 72
7 → 14 → 56
6 → 12 → 42
5 → 10 → 32
4 → 8 → 24
3 → 6 → 18

Fixed - Bias Config :-

$$S(I_{CO}) = \beta + 1 \qquad (4.58)$$

Feedback - Bias Config :-

$$S(I_{CO}) = (\beta+1)\cdot\frac{(1+R_B/R_C)}{(\beta+1)+R_B/R_C} \qquad (4.6)$$

Construction & Characteristics of JFETs :-

Voltage Control Resistor :-

$$r_d = \frac{r_o}{(1-V_{GS}/V_P)^2} \qquad (5.1)$$

where, r_o is the resistance with $V_{GS} = 0V$

r_d = The resistance at a particular level of V_{GS}.

P - Channel Devices :-

I_D vs V_{GS} Graph:-

Shorthand Method:-

V_{GS} versus I_D using Shockley's Equation

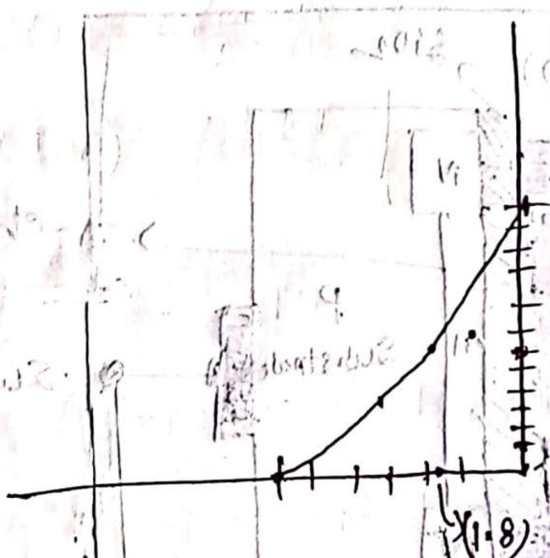
V_{GS}		I_D
0	→	I_{DSS}
$0.3\ V_P$	→	$I_{DSS}/2$
$0.5\ V_P$	→	$I_{DSS}/4$
V_P	→	0 mA

Example:- Sketch the Transfer curve defined by $I_{DSS} = 12\ mA$ and $V_P = -6V$.

Solution:-

POI-0

$I_{DSS} = 12\ mA$ and $V_{GS} = 0V$



By using Shockley's equation

$I_{DSS} \rightarrow 0 = I_{DSS}$

$I_{DSS}/2 \rightarrow 0.3 V_P = 6 \times 0.3$

$I_{DSS}/4 \rightarrow 0.5 V_P = 6 \times 0.5$

$0 mA \rightarrow V_P = 0 mA$

Depletion – Type MOSFET :-

MOSFETs are Further broken down into depletion type and enhancement type. The terms depletion and enhancement define their basic mode of operation. MOSFET stands for Metal-Oxide-Semiconductor Field-effect transistor. Since there are differences in the characteristics and operation of each type of MOSFET, they are covered in seperate sections.

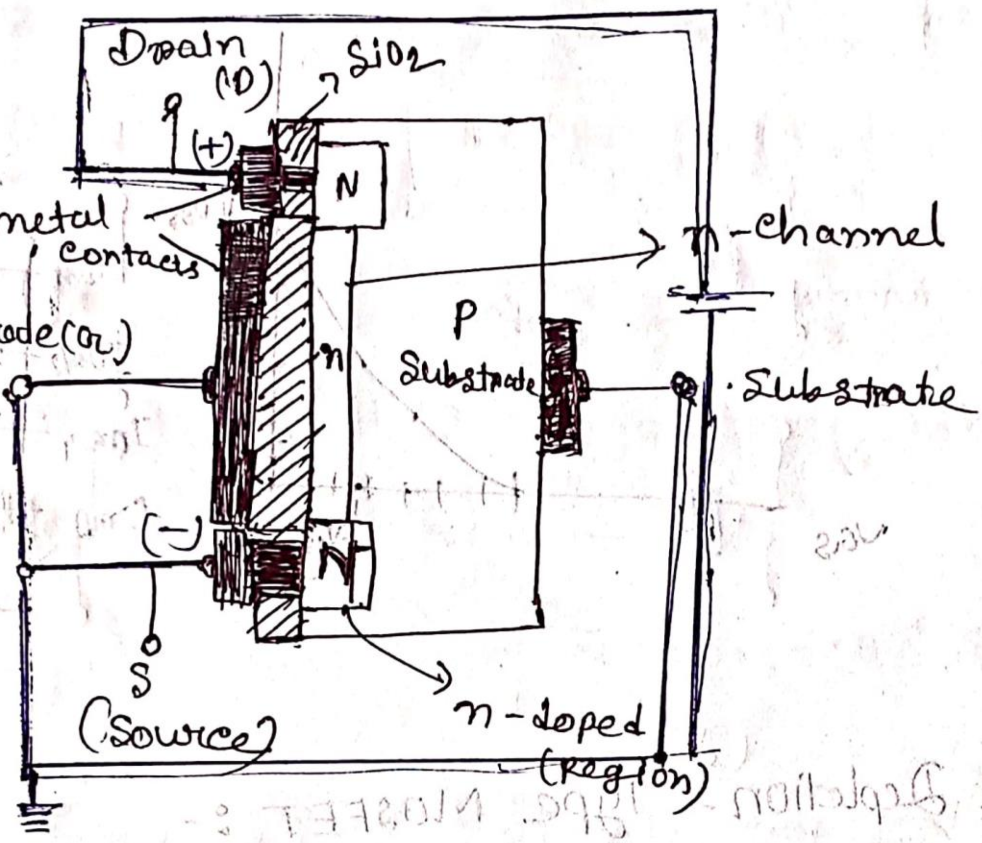


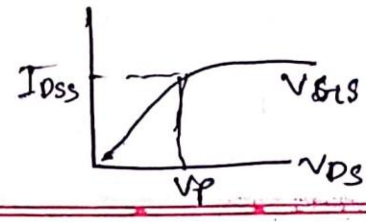
Figure: n-channel depletion type MOSFET

=> metal contacts বলা হয় কারণ উপরে ও নিচের Materials দুয়কে Metallic ভাবে Connect করা হয়েছে।

=> N channel ও gate এর মাঝে SiO_2 এর একটি Layer থাকে। একারনে একে Oxide বলে।

=> এটি একটি Semi Conductor device ও

=> আর এখানে দেওয়া voltage এর সাথে Drain Current এর কোনো সংযোগ নেই একারনে এটি



Field Effect Transistor বলে।

উপরোক্ত বর্ণনাটি (MOSFET) এর।

operation of MOSFET (কাজ):-

উপরোক্ত Figure এ (+) terminal n-type এর electron গুলোকে আকর্ষণ এবং (-) terminal electron গুলোকে ধাক্কা দিবে এর ফলে electron Flow এর একটি পথ হবে।

votage যত বাড়বে ohm's law অনুযায়ী electron Flow বাড়বে। একসময় N-channel এর ধারনক্ষমতা পূর্ণ হবে। ফলে যতই voltage বাড়ানো হোক electron pass আর হবে না।

আর Negative যদি (Gate) এ দেওয়া হয় তখন বিকর্ষণ তৈরি হয় electron - electron

MOSFET কে Depletion type এ ব্যবহার করা হয়। যেহেতু সবসময় Depletion type এ ব্যবহার করা হয় তাই MOSFET কে Depletion Type Transistor ও বলা হয়।

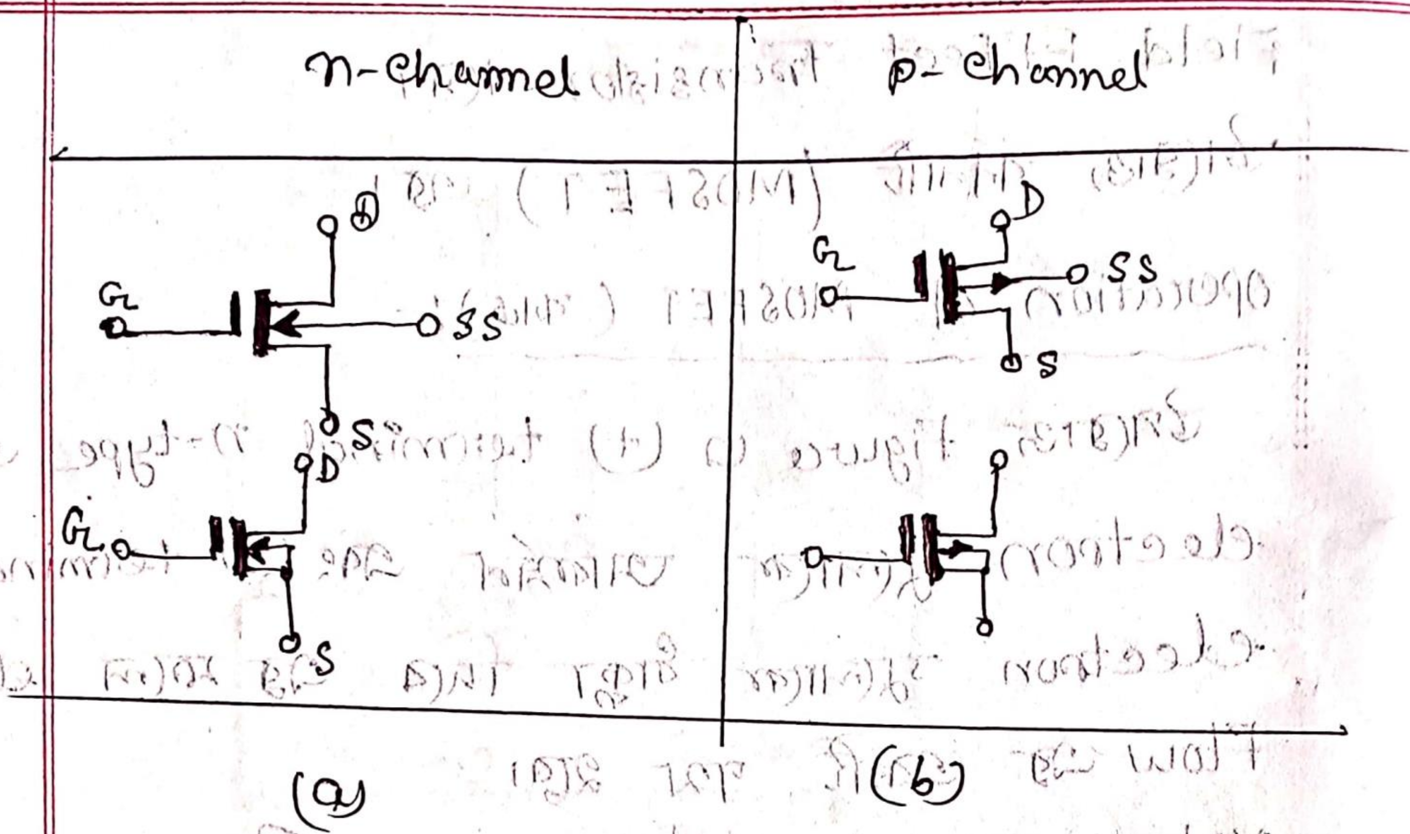
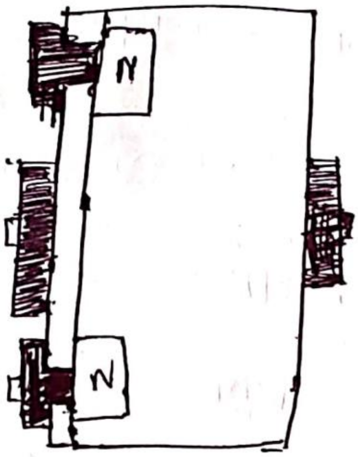


Figure:- Graphic Symbols for (a) n-channel depletion-type MOSFETs and (b) P-channel depletion-type MOSFETs

Enhancement MOSFET :-

এখানে কোনো n-channel নাই।



Question & answer :-

(1) $\begin{cases} V_{CE} = V_{CC} - I_C R_C \\ I_C = \dfrac{V_{CC}}{R_C} \end{cases}$

$\beta = 80$

$S(I_{CO}) =$